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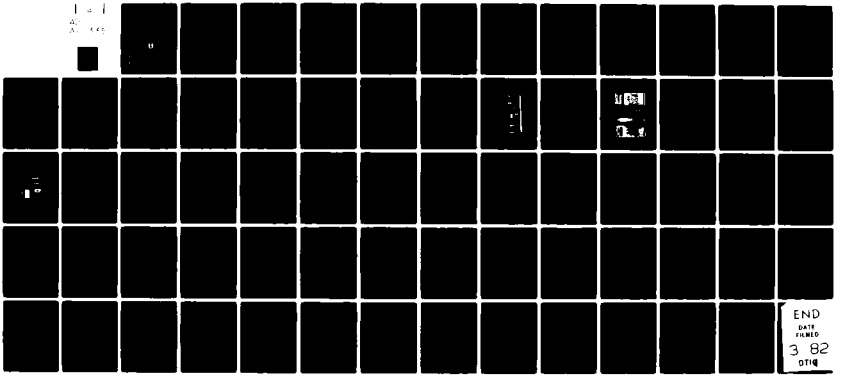

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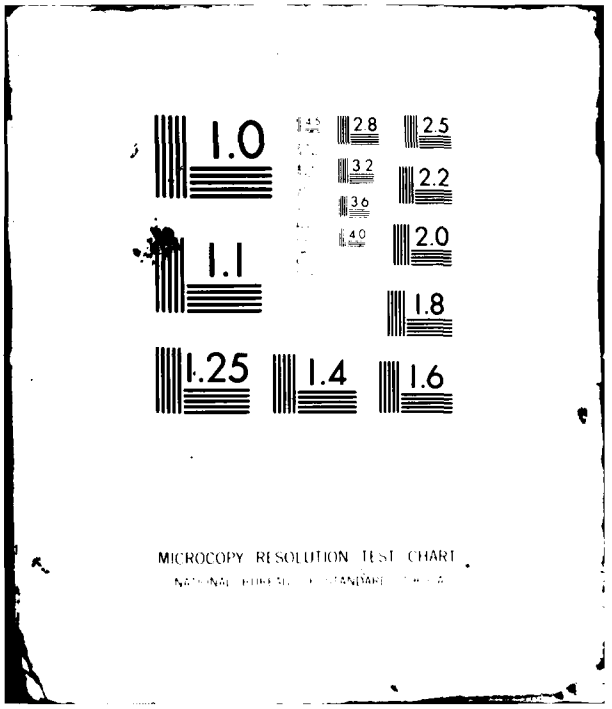
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CCD MULTI-FUNCTION PROCESSOR TEST BED

By

M. W. Paczan
and
S. M. Waldstein

JANUARY 1982

Prepared for

DEPUTY FOR ELECTRONIC TECHNOLOGY
ELECTRONIC SYSTEMS DIVISION
AIR FORCE SYSTEMS COMMAND
UNITED STATES AIR FORCE
Hanscom Air Force Base, Massachusetts

Project No. 7170

Prepared by

THE MITRE CORPORATION
Bedford, Massachusetts
Contract No. F19628-81-C-0001

REVIEW AND APPROVAL

This technical report has been reviewed and is approved for publication.

Jerry Silverman

JERRY SILVERMAN
Project Engineer

Freeman D. Shepherd

FREEMAN D. SHEPHERD, Chief
Electronic Device Technology Branch
Solid State Sciences Division

FOR THE COMMANDER

Harold Roth

HAROLD ROTH, Director
Solid State Sciences Division

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REPORT DOCUMENTATION PAGE		READ INSTRUCTIONS BEFORE COMPLETING FORM
1. REPORT NUMBER ESD-TR-81-394	2. GOVT ACCESSION NO. AD-A111 335	3. RECIPIENT'S CATALOG NUMBER
4. TITLE (and Subtitle) CCD MULTI-FUNCTION PROCESSOR TEST BED		5. TYPE OF REPORT & PERIOD COVERED 6. PERFORMING ORG. REPORT NUMBER MTR-8417
7. AUTHOR(s) M. W. PACZAN S. M. WALDSTEIN		8. CONTRACT OR GRANT NUMBER(s) F19628-81-C-0001
PERFORMING ORGANIZATION NAME AND ADDRESS The MITRE Corporation P. O. Box 208 Bedford, MA 01730		10. PROGRAM ELEMENT, PROJECT, TASK AREA & WORK UNIT NUMBERS Project No. 7170
11. CONTROLLING OFFICE NAME AND ADDRESS Deputy for Electronic Technology Electronic Systems Division, AFSC Hanscom Air Force Base, MA 01731		12. REPORT DATE JANUARY 1982 13. NUMBER OF PAGES 74
14. MONITORING AGENCY NAME & ADDRESS(if different from Controlling Office)		15. SECURITY CLASS. (of this report) UNCLASSIFIED 15a. DECLASSIFICATION DOWNGRADING SCHEDULE

16. DISTRIBUTION STATEMENT (of this Report)

Approved for public release; distribution unlimited.

17. DISTRIBUTION STATEMENT (of the abstract entered in Block 20, if different from Report)

18. SUPPLEMENTARY NOTES

19. KEY WORDS (Continue on reverse side if necessary and identify by block number)

ADAPTIVE CHANNEL EQUILIZATION
CCD
FILTERS
PROGRAMMABLE TRANSVERSAL FILTER
SPREAD SPECTRUM

20. ABSTRACT (Continue on reverse side if necessary and identify by block number)

This report describes the Charge-Coupled Device (CCD) Multi-Function Processor Test Bed developed to support the test and evaluation of, and experimentation with, second- and third-generation CCD Programmable Transversal Filters (PTF) developed for RADC/ESE by Texas Instruments. Application of the CCD PTF as an adaptive equalizer for a wideband HF system and a matched filter for a spread-spectrum modem are discussed.

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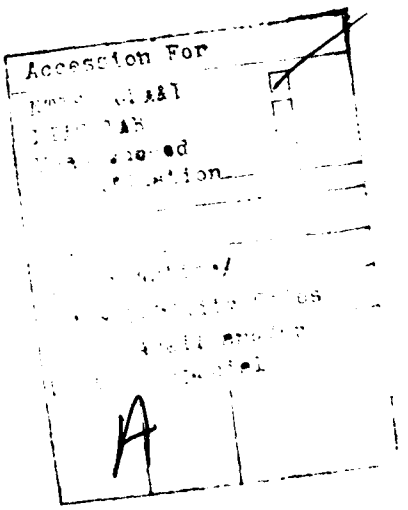
EXECUTIVE SUMMARY

A test bed was developed to support the test and evaluation of, and experimentation with the Texas Instruments CCD PTFs. The test bed consists of the PTF Module and PTF Exerciser Module. These modules provide the circuitry necessary to program, operate, control, and interface the PTF device.

Experimental measurements made on the PTF in our laboratory have confirmed the published results of Texas Instruments. The present level of performance justifies continued experimentation and investigations into applications of the PTF as a generic signal processing module. Two areas that will continue to be pursued in FY82 include comparing the performance of the PTF configured as an adaptive equalizer in a wideband HF system against an existing all-digital equalizer and, secondly, application of several PTF Modules as a matched filter in a spread-spectrum modem. The modular construction of the PTF Test Bed is well suited to support these and other potential applications.



ACKNOWLEDGMENTS

This report has been prepared by The MITRE Corporation under Project 7170. The contract is sponsored by the Electronic Systems Division, Air Force Systems Command, Hanscom Air Force Base, Massachusetts.

The authors wish to acknowledge the efforts of others who contributed to the work described in this paper. G. L. Glatfelter, S. Meehan, D. R. Bungard, and W. Ewing (RADC/ESE) were extremely helpful with the development of the modular concept and actual circuit implementations. C. Phillips, J. J. Sawyer, E. H. Gelin, and K. Gordon built the equipment. J. Low, J. E. Blanchard, W. M. Bridge, and M. A. Poole all contributed to the design concept used for the spread-spectrum modem. B. D. Perry developed the HF equalization concept outlined in Section 4 and H. E. T. Connell and L. Lau assisted in the development of the equalizer test bed. Additionally, T. J. McDonald provided excellent support for the documentation phase of this work. Finally, we would like to thank RADC/ESE for the developmental CCDs provided which made this work possible.

TABLE OF CONTENTS

LIST OF ILLUSTRATIONS

LIST OF TABLES

SECTION 1

INTRODUCTION

1.1 PURPOSE

The purpose of this report is to describe the Charge-Coupled Device (CCD) Multi-Function Processor Test Bed developed under the LSI Signal Processing Project. The test bed supports the test and evaluation of, and experimentation with, second- and third-generation CCD Programmable Transversal Filters developed for RADC/ESE by Texas Instruments.

1.2 BACKGROUND

The increasing demand for system performance, which drives increasing complexity of computational algorithms, has resulted in the need for high-speed, specialized, complex signal processing components. These components, not feasible only a few years ago, can exist today due to recent advances in large-scale integrated (LSI) circuit technology. The advances in monolithic circuit technology can reduce the expanding system complexity (and life-cycle cost) by absorbing the processing complexity in functionally definable hardware modules. Such functional blocks can be generic; their application is not confined to a particular problem or system. The cost of their design and development can therefore be dispersed over a potentially wide base, a concept central to the emerging DOD-sponsored Very High Speed Integrated Circuit (VHSIC) program.

The LSI Signal Processing Project endeavors to promote the development and application of advanced LSI circuits for use in

military electronic systems through analysis and experimentation in specific signal and data processing areas. Emphasis is on the realization of new capabilities, improved system performance, and reduced system cost for command, control, and communication (C^3) systems through exploitation of emerging LSI signal processing devices and technology. The program is concurrent with the technological advances of the VHSIC program, and complements the technology of that long-term project with the application of devices that have near-term impact. Current project activities have focused on the application of available state-of-the-art signal processing technology and devices, logic circuits, and reconfigurable CCD processors to achieve needed signal processing throughput.

CCDs have matured into self-contained signal processing functional blocks that can influence future system architecture and design. Work previously completed under the MOIE program included the testing of developmental CCD processors for linear signal processing. The work included laboratory tests and measurements on single first-generation devices delivered to RADC/ESE under its electronic device development program. MITRE's work was directed toward understanding the devices and their practical limitations as a prerequisite to the design of full-function C^3 signal processors.

Currently, under the Advanced Signal Processing Devices Task of Project 7170, MITRE is evaluating the application of advanced CCD signal processors being developed for RADC/ESE by Texas Instruments (TI) and RCA. One device is a programmable multi-function transversal filter capable of performing a set of mission-oriented signal processing functions that include pseudo-noise (PN) sequence matched filtering, adaptive channel equalization, and adaptive pre-whitening filtering. The other devices are designed to perform PN-sequence matched filtering and signal integration.

The CCD Multi-Function Processor Test Bed was developed to operate the TI programmable multi-function transversal filter (PTF) and support, through experimentation, the evaluation of the device characteristics and limitations in signal processing applications. Future work will include applying the PTF as an adaptive channel equalizer.

1.3 SCOPE

This report is divided into three principal sections and two appendices. Section 2 describes the Texas Instruments CCD PTF. The section includes a general discussion of the device architecture, configurations, programmability, and performance. Section 3 provides a general functional description of the modules which constitute the test bed and a discussion of the test bed system operation. Current and planned test bed applications and experimentation are discussed in section 4. Appendix A provides a detailed description of the test bed circuits and operation. Appendix B lists the procedure for test bed set-up.

SECTION 2

CCD PTF DESCRIPTION

The central element of the CCD multi-function processor is a general-purpose, 1024-stage, binary/analog programmable transversal filter implemented in n-channel metal-oxide-semiconductor (NMOS) technology. The PTF device was designed and fabricated by Texas Instruments under Contract F10628-78-C-0122, "Binary/Analog CCD Correlator Development," to the Deputy for Electronic Technology, Rome Air Development Center at Hanscom AFB, MA. (references 1 and 2). The filter features electronic programmability of the reference signal, filter length, and weighting coefficient resolution. These features are programmed under external user/microprocessor control, resulting in a flexible monolithic analog signal processing system that can be operated in nine programmable configurations.

2.1 GENERAL ARCHITECTURE

The architecture of the programmable transversal filter is shown in the simplified block diagram of figure 1. The major functional elements of the device are the input scaling network, input switching, CCD differential tapped delay line and dynamic shift register array, the differential current integrators (DCIs), output signal weighting, and peripheral control circuitry. The key element is the 4-phase, 1024-stage-CCD filter array which is partitioned into eight, 128-stage transversal filter sections with 1-bit weighting coefficients. Input switches determine the selection and routing of the input signals to the eight elemental filter sections and, along with the output switches, set the PTF mode of operation. Signal scaling is performed at the input and output to achieve an optimum balance between multiple-bit accuracy, circuit complexity,

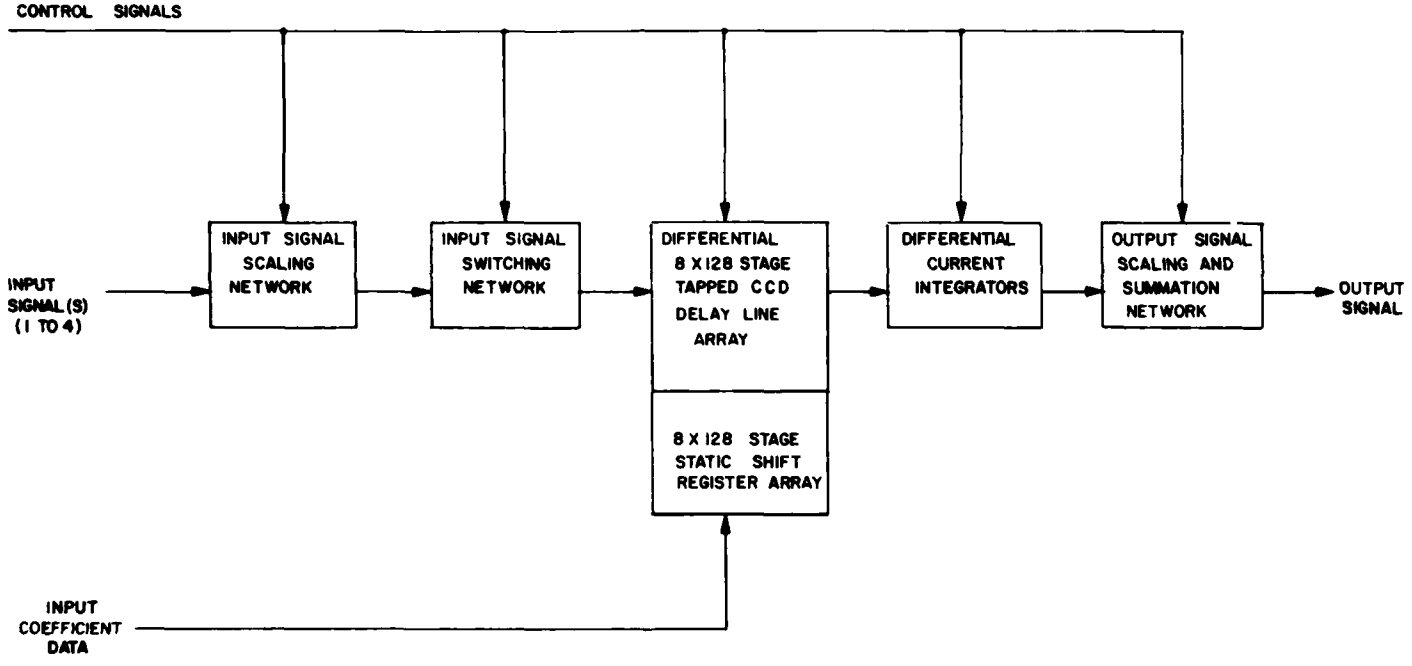


Figure 1. CCD PTF Functional Block Diagram

and dynamic range. Each 128-stage CCD filter section is constructed with two, parallel, 128-stage CCDs which form a differential channel. A differential channel is used to eliminate DC offset, which is dependent on the filter weighting coefficients, and therefore to minimize the impact of this offset on dynamic range. Additional control logic is provided in the device for clock generation, mode selection, and microprocessor interface circuitry.

2.2 CONFIGURATIONS

Nine filter configurations are permitted by altering the physical interconnection of the eight elemental filter units. As shown in figure 2, switches S1 through S10 control the interconnection of the filter sections and, therefore, the filter length, along with the amount of input and output signal scaling. A 4-bit input word to the PTF allows the user to select the filter mode by electronically altering the position of the input and output switches. The nine modes of operation are summarized in table 1.

2.3 PROGRAMMABILITY

The weighting coefficients (h_n) of a transversal filter can be decomposed into the two's complement binary/analog representation:

$$h_n = -h_n^o + \sum_{k=1}^{M-1} h_n^k \; 2^{-k}$$

where h_n^k is either 0 or 1 and 2^{-k} is the scale factor for the particular bit.* For M-bit accuracy of each weighting coefficient, M parallel CCD binary/analog filters are required. To obtain electronic programmability, the PTF device is constructed with a

*For more detailed background information on transversal filters references 3 and 4 are recommended.

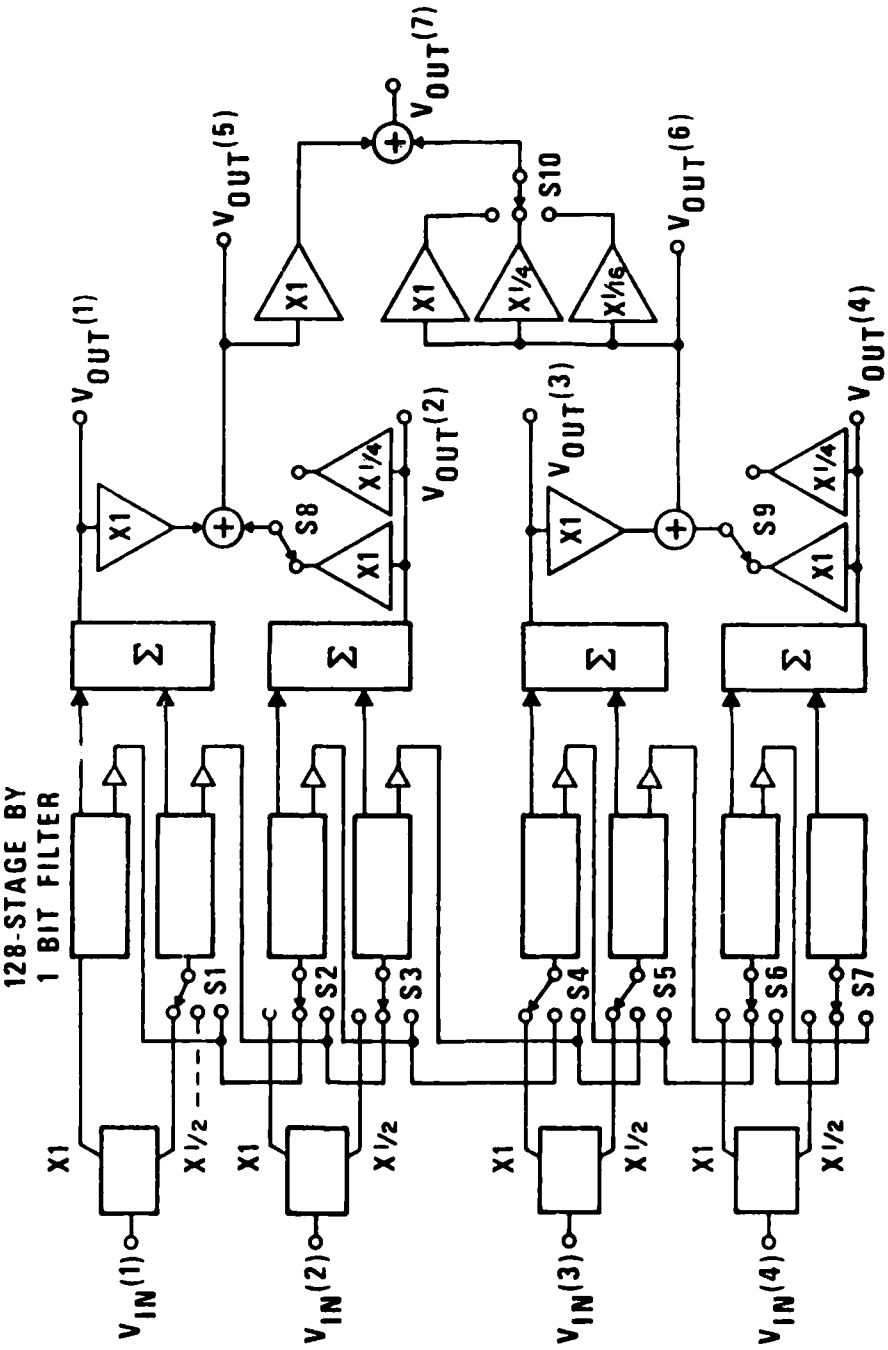


Figure 2. PTF Element Structure

(Excerpted from reference 1, courtesy of Texas Instruments)

Table 1

PTF Modes of Operation

Mode Number	Filter Length	Coefficient Word Length	Number of Filters
1	1024-stage	1-bit	1
2	512-stage	2-bits	1
3	256-stage	4-bits	1
4	128-stage	8-bits	1
5	512-stage	1-bit	2
6	756-stage	2-bits	2
7	128-stage	4-bits	2
8	256-stage	1-bit	4
9	128-stage	2-bits	4

shift register array that can be loaded with the binary values h_n^k. The values in the shift registers represent a coefficient tap weight and are used to control the relative timing of charge transfer to the sense electrode in the 4-phase CCD registers.

This structure is functionally depicted in figure 3 where the elongated rectangles represent the shift registers and the squares (marked D) represent the CCD register stages. For static shift register stages loaded with $h_n^k = 0$, the charge in the corresponding CCD stage, representing the sampled analog input signal, is transferred early in the CCD cycle so that it contributes to the DCI output. If $h_n^k = 1$, the charge is transferred after the integrator sampling period is over, and therefore does not contribute to the DCI output.

2.4 PERFORMANCE

The performance of the CCD-based transversal filter has been evaluated by measuring the input dynamic range, charge transfer inefficiency (CTI), output DC offset due to tap weight coefficients (code dependent bias), coefficient accuracy, tap weight linearity, tap weight dynamic range, and maximum sampling frequency for several generations of devices. The independent measurements made in our laboratory confirm the published results of Texas Instruments (reference 1).

The input dynamic range was measured to be greater than 70 dB with a sensitivity of less than 1 mV and the CTI was 1.3×10^{-3}/stage. The code dependent offset was less than 30 mV for a change in tap weight coefficients of all 1's to all 0's. These results are better than the 50 mV offset measured by TI. The tap weight accuracy was measured to be 0.2%, which is consistent with

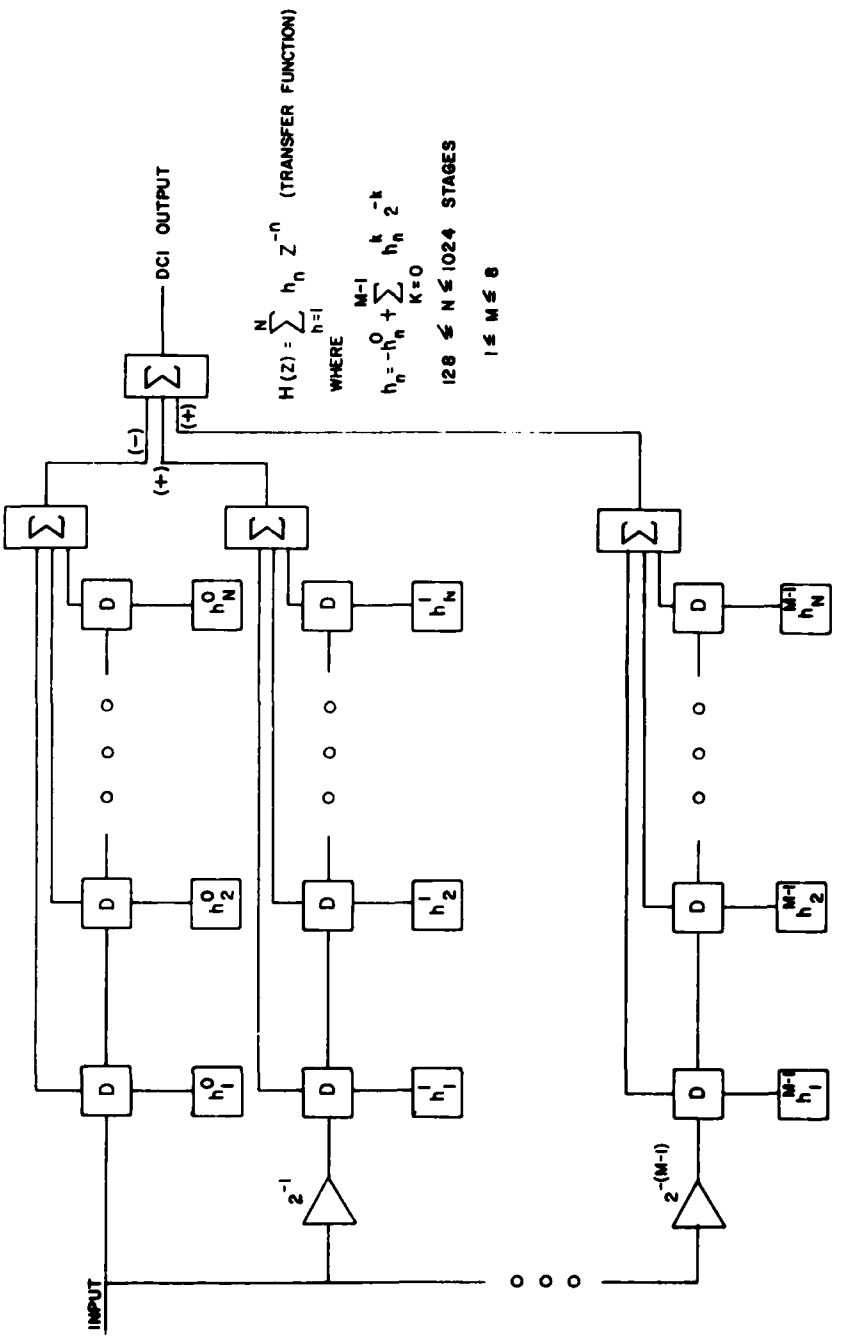


Figure 3. Programmable Filter Array Structure

8-bit coefficients. The linearity of the tap weights was within 1% of -40 dB RMS error over the entire Nyquist bandwidth ($0\text{-}F_c/2$). The dynamic range per tap was determined by measuring the peak RMS signal to RMS noise voltage over a 50 kHz bandwidth. The measured dynamic range was 32 dB with a peak RMS signal of 40 mV per tap and a $2\ \mu V/\sqrt{Hz}$ or 1 mV RMS noise voltage over 50 kHz. The maximum sampling frequencies measured for the PTF/1 and the PTF/2 were 850 kHz and 700 kHz, respectively. The maximum sampling frequency for the PTF/3 was 870 kHz.*

* PTF/1, PTF/2, and PTF/3 refer to the first-, second-, and third-generation TI experimental programmable transversal filters.

SECTION 3

TEST BED FUNCTIONAL DESCRIPTION AND OPERATION

3.1 INTRODUCTION

The PTF test bed (figure 4) allows flexibility in reconfiguring the TI PTF device to support experimental signal processing configurations and measurement of CCD device parameters. Flexibility is achieved through a modular hierarchical test bed system which presently consists of two principal elements: the CCD PTF Module and the PTF Exerciser Module.

The CCD PTF Module represents the fundamental element of the test bed. It incorporates the circuitry to interface the input, output, and control signals with the PTF; and to develop the necessary bias voltages for proper device operation. The second modular element, the PTF Exerciser Module, performs the control function for the test bed, permits manual selection of the filter mode and coefficients, and provides the master clock and clock synchronizing circuitry to operate two PTF devices in tandem. This module can be replaced by logic components, such as a microcomputer, which will permit rapid automatic reconfiguration of the PTF device.

3.2 PTF MODULE

The CCD PTF Module contains the circuitry necessary to operate and interface the TI PTF/3 device with external inputs, outputs, control equipment and power supplies. A functional block diagram and a photograph of the module are shown in figures 5 and 6.

The input switches control the input signal routing for the several PTF modes of operation. The switches permit the following input options:

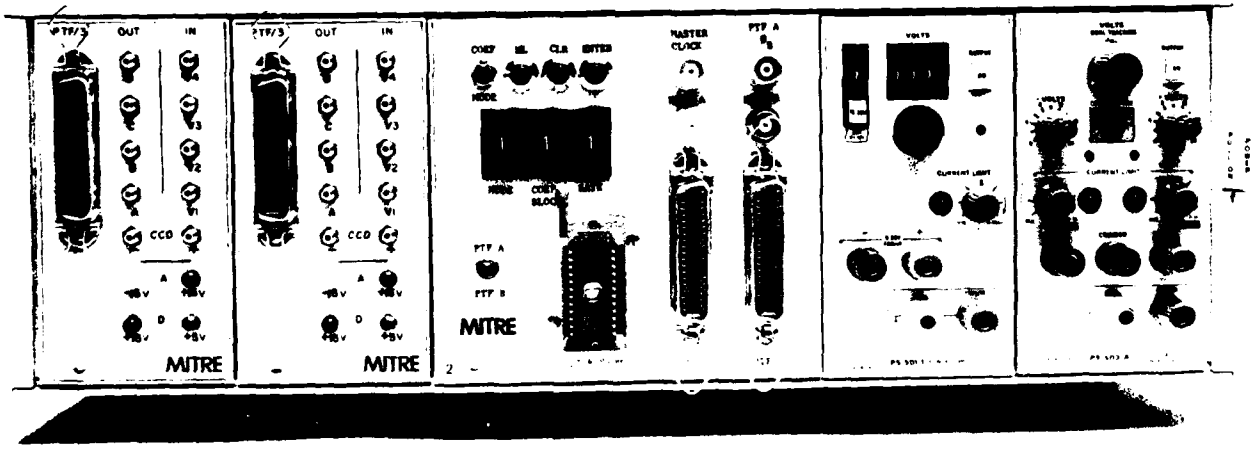


Figure 4. PTF Test Bed

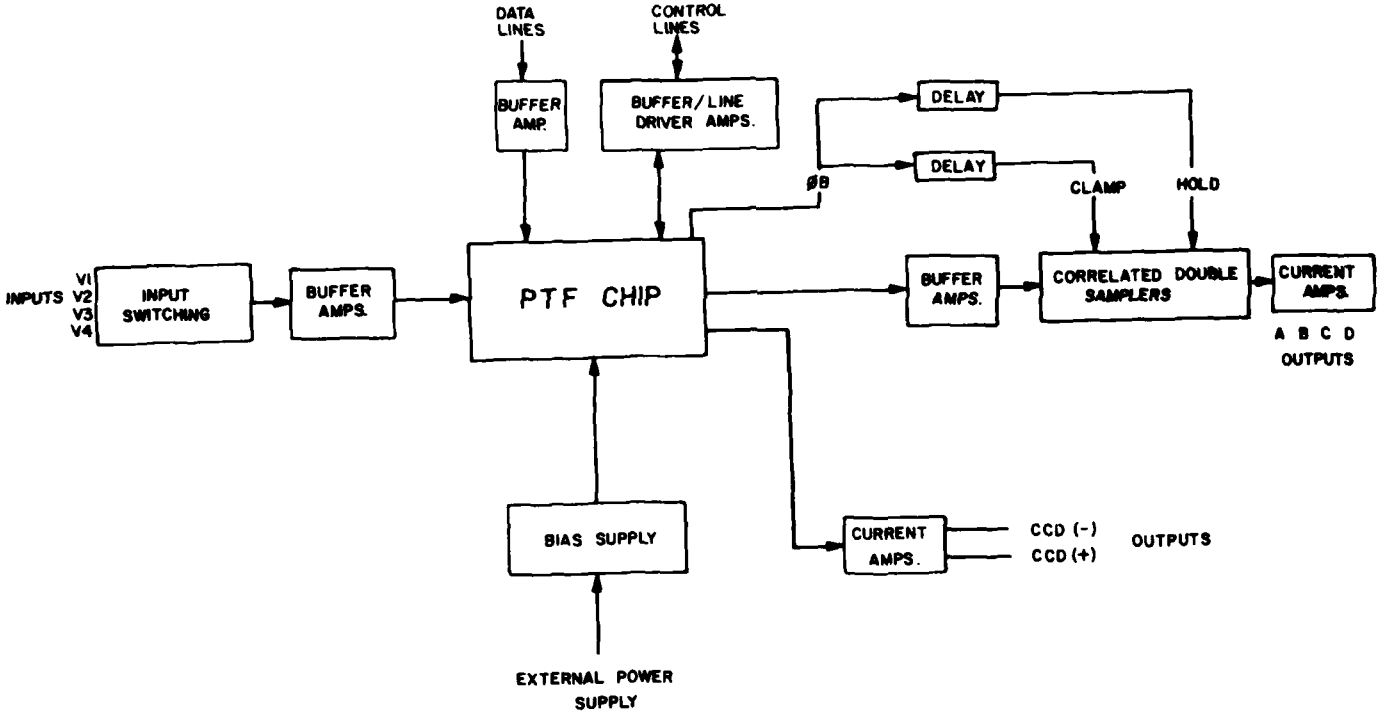


Figure 5. PTF Module Functional Block Diagram

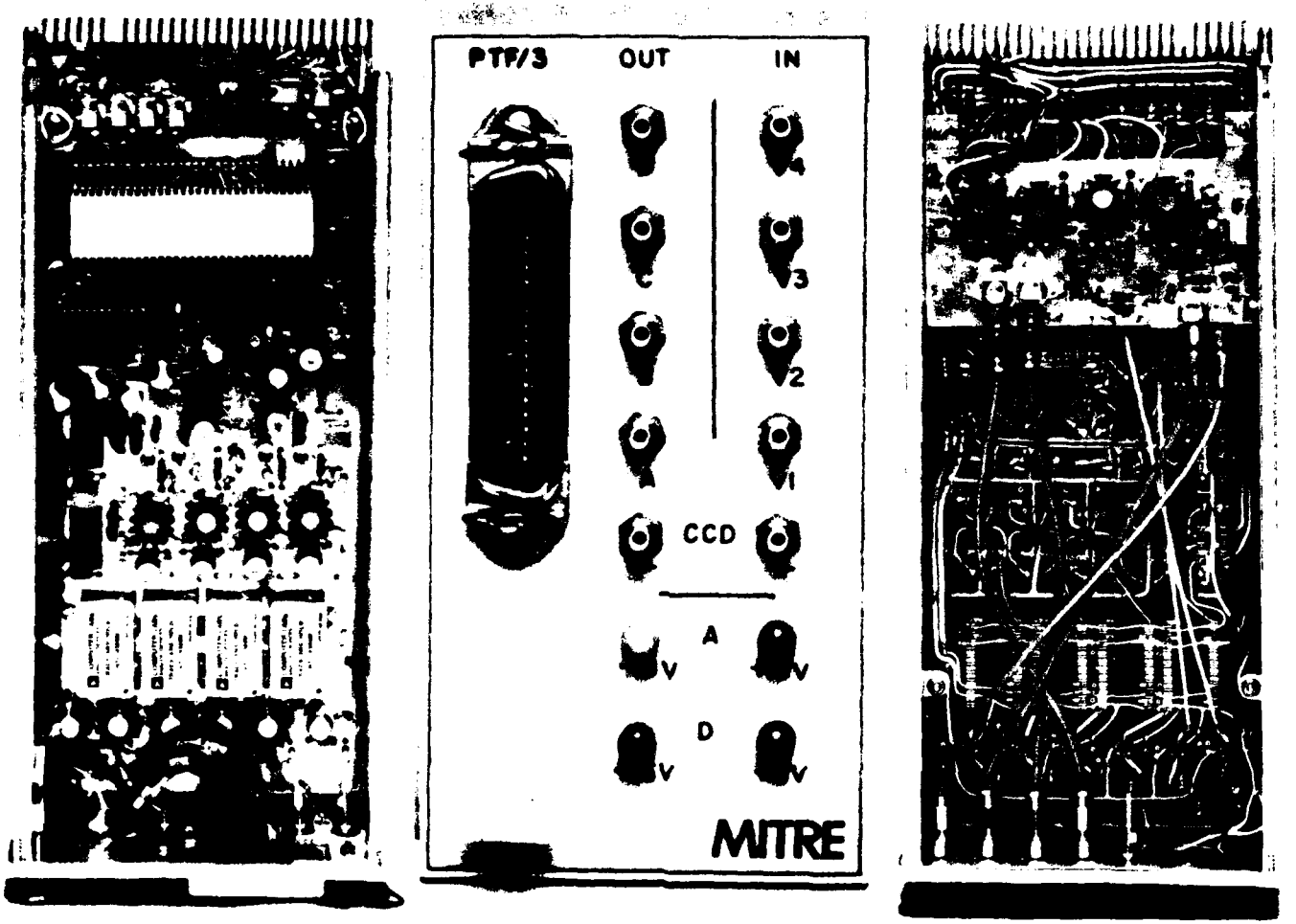


Figure 6. PTF Module Front and Internal Views

1. same signal connected to all four CCD inputs (Single Mode),
2. one input shared between $V_{in}(1)$ and $V_{in}(2)$ and another input shared between $V_{in}(3)$ and $V_{in}(4)$ (Dual Mode), and
3. separate signals connected to each of the four CCD inputs (Quad Mode).

The input switches are followed by amplifiers that buffer the CCD input and adjust the DC level to interface bipolar signals into the PTF device.* The output of the PTF is also buffered by non-inverting unity gain operational amplifiers to supply a high impedance input for the correlated double sampler (CDS). The CDS eliminates the output DC reference voltage of the PTF DCIs; it also tracks and holds the desired CCD analog output signal during the appropriate time interval. Proper sample time is controlled by the two delay elements which set the time for the clamp-and-hold control signals to the CDS. Current amplifiers on the output allow the PTF module to be interfaced to external equipment.

Two additional outputs, CCD (-) and CCD (+), are available from the PTF device and are interfaced with external equipment via current amplifiers. Other peripheral circuitry includes buffer amplifiers and line drivers for the digital DATA and CONTROL lines and adjustable voltage divider circuits to set the device voltage bias levels.

3.3 PTF EXERCISER MODULE

The PTF Exerciser Module performs the control and programming functions for the PTF test bed. As shown in figure 7, the module consists of several functional blocks which operate to select and

* This DC level adjustment is necessary since CCD devices are inherently unipolar.

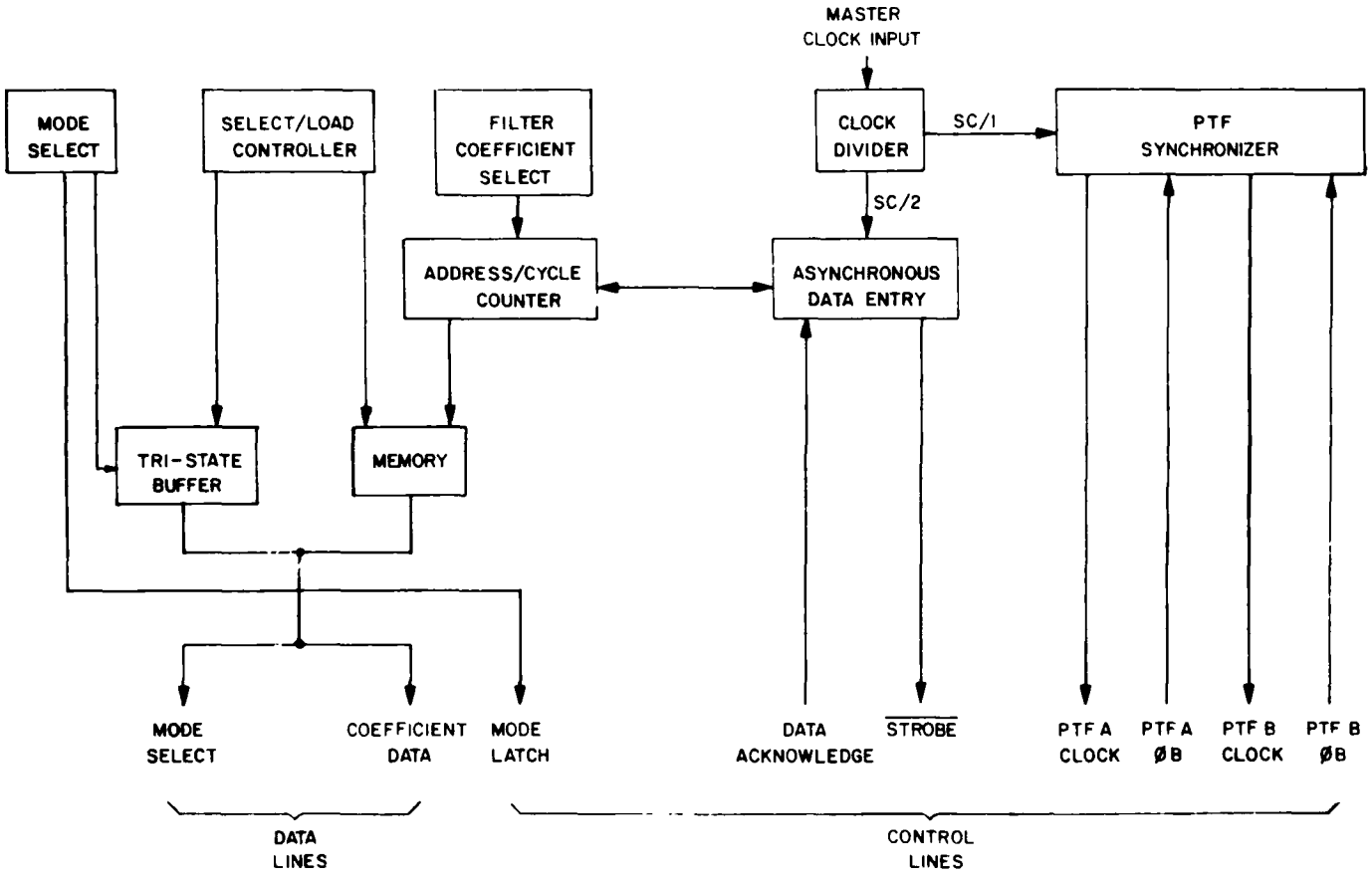


Figure 7. PTF Exerciser Module Functional Block Diagram

enter the filter mode and coefficients, set the coefficient load rate, and route the PTF A/B timing/control signals for single or tandem PTF operation. User control of these functions is facilitated by the front panel switches pictured in figure 8.

The coefficient/mode load selector functions to select whether the filter mode or coefficients are entered into the PTF Module by establishing control signals to the tri-state buffer and memory chip. The mode select, when permitted by the coefficient/mode load selector, will allow selection and entering of any of the nine filter modes by sending a 4-bit code word to the PTF via the tri-state buffer. Similarly, the filter coefficient select will allow selection and entering of the filter binary weighting coefficients by establishing control signals to the address/cycle counter. The address/cycle counter addresses any one of eight blocks of 128 x 8 bits of memory and will output the coefficients to the DATA lines. This control arrangement for the mode and coefficients is necessitated by the sharing of four of the output data lines between the mode select circuitry and the coefficient select circuitry.

The clock divider functions to derive several system clocks from the master clock input. These system clocks control the entry of programming data to and the timing of the PTF devices. The clock divider first divides the master clock input by the fixed factor of two. This system clock (SC/1) is used as the master clock input to the PTF device. The clock rate is further reduced by a variable

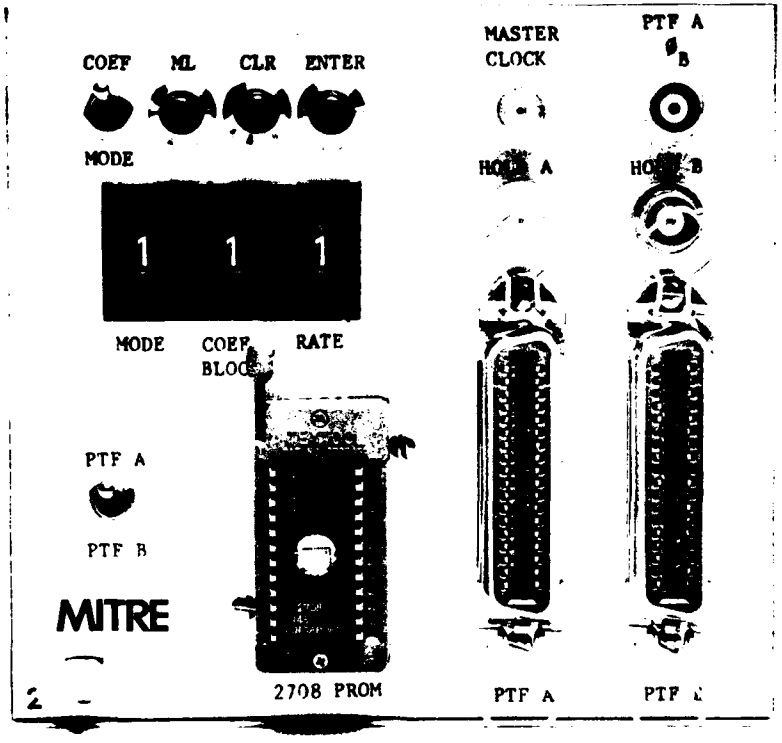


Figure 8. PTF Exerciser Module Front Panel

factor of N+1, under control of the front panel RATE thumbwheel. This system clock (SC/2) drives the clock input to the address/cycle counter and therefore permits limited control over the coefficient load rate. To operate at the PTF rate limit, the master clock input is 8 MHz. The generated SC/1 clock would then be 4 MHz, corresponding to the maximum 4-phase CCD cycle time of 1 MHz.

The ϕ_B (phase B) synchronizer allows the test bed to be configured to support complex filter configurations requiring two PTF Modules. The synchronizer locks up the PTF A and PTF B clocks based on a ϕ_B input from each PTF Module.

3.4 SYSTEM OPERATION

The test bed permits the implementation of a signal processing function through a sequence of interactive operations that occur between the PTF Module and the PTF Exerciser Module. Figure 9 illustrates the signal flow for these operations. The following sections provide a general description of module interface operations, while detailed test bed set-up instructions are described in Appendix B. When the set-up operations are complete, the PTF device will process the analog input signals on a continuous basis.

3.4.1 Mode Load

The first sequential test bed operation is mode load. The 4-bit code word representing the mode is generated by the mode select circuitry and routed via the tri-state buffer and output data lines into the PTF device. A latch pulse, activated by a front panel switch on the PTF Exerciser Module, will cause the PTF device to enter the mode data and prevent further changes on the data lines from affecting the mode.

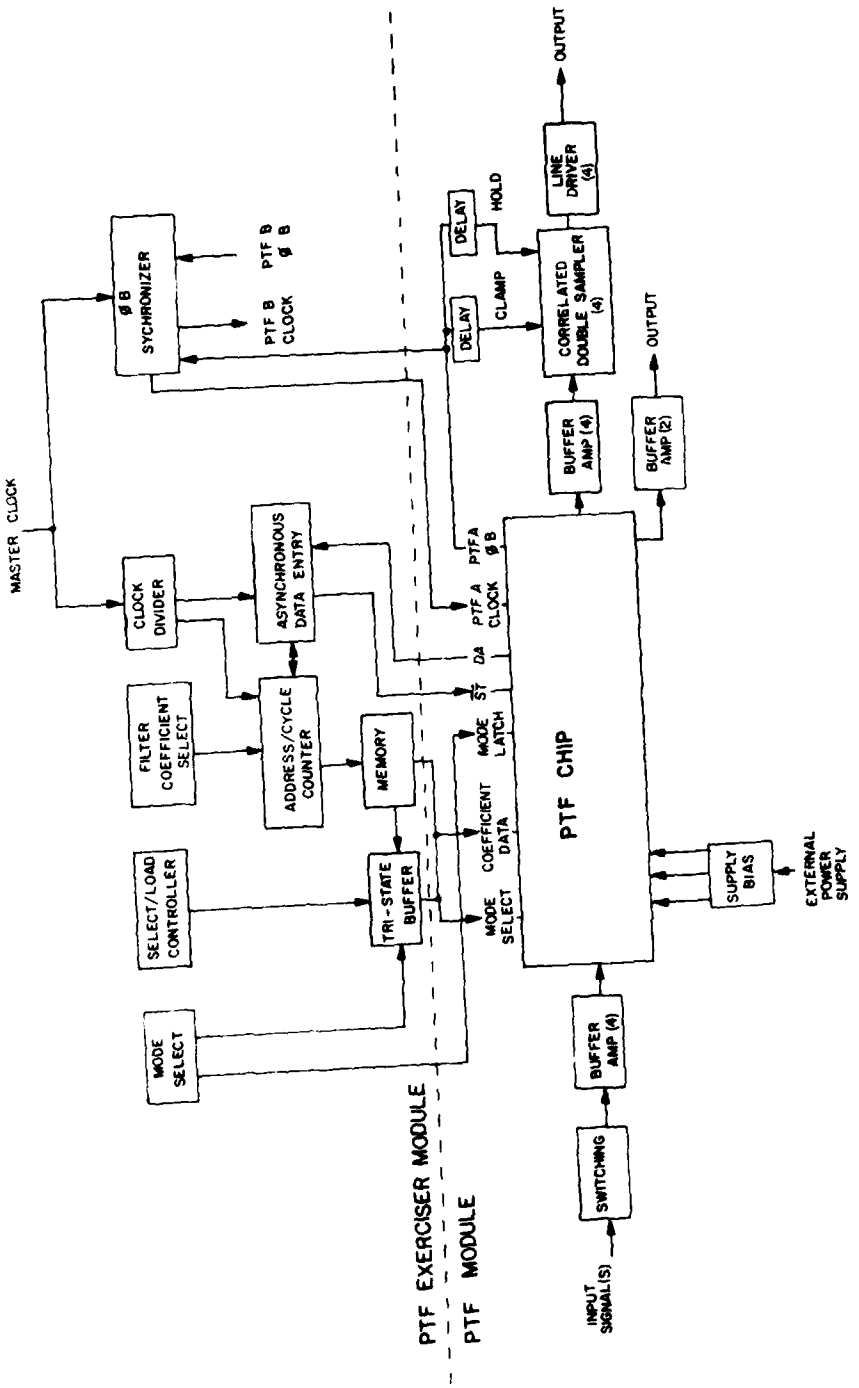


Figure 9. PTF Test Bed Functional Block Diagram

3.4.2 Coefficient Load

The next sequential operation is coefficient load. The first 8-bit word of the desired block in memory is addressed and a strobe pulse generated by the asynchronous data entry (ADE) circuit notifies the PTF device that data is available. The PTF responds with a data acknowledge (DA) high signal to the asynchronous data entry circuit indicating that the PTF will enter the 8-bit coefficient word on the next appropriate CCD clock phase. When the coefficient has been entered, a DA low signal will indicate to the asynchronous data entry circuit that the next coefficient can be addressed for entry. The asynchronous data entry circuit will now clock the address/cycle counter to the second 8-bit word in memory and the process will repeat until all 128, 8-bit words have been entered.

3.4.3 Tandem PTF Synchronization

To operate two PTF devices in tandem, their internal clock cycles must be synchronized. The PTF synchronizer continuously compares the $\emptyset_B$ signal outputs from two PTF devices and functions to delay the PTF B system clock for one cycle if the two $\emptyset_B$ signals do not occur simultaneously. The process of stopping the PTF B clock for one cycle and comparing $\emptyset_B$ signals continues until the PTF A and PTF B $\emptyset_B$ signals are synchronized.

SECTION 4

MODULE APPLICATION AND EXPERIMENTATION

4.1 GENERAL

Transversal filters* can satisfy a number of signal processing requirements. These include frequency selective filtering, matched filtering for communications and radar, and adaptive filtering. The electronic programmability of the PTF permits its use as a multi-function processor which can be reconfigured in real time to support different signal processing functions. As a generic signal processing module it can support several mission-oriented tasks with a minimum of hardware duplication.

For example, it is plausible to have one or two filter modules as part of an aircraft communication system perform the following functions:

- o pre-whitening of the communication signal,
- o matched filtering in the receiver,
- o linear prediction in a low bit rate speech coder,
- o adaptive equalization of the communication channel, and
- o out-of-band jammer suppression.

The reduced hardware requirements would improve reliability, maintainability, and reduce system cost.

The application limitations are a direct function of the device operating characteristics. Device bandwidth, reconfiguration time,

* Also known as finite impulse response (FIR) filters.

dynamic range, coefficient word length, CCD filter length and time-bandwidth product are several of the more important parameters which impact system applicability.* These areas are currently being investigated in Project 7170 through device measurements and prototype system experiments. Two applications currently being investigated include using the PTF as an adaptive equalizer for a wideband HF communications system and as matched filters for a spread-spectrum modem. The modular construction of the PTF Test Bed is well suited to support these and other potential applications.

1.1 ADAPTIVE EQUALIZER

Adaptive filtering for channel equalization is an important system application for the PTF Module. Previous work conducted under MITRE Project 7140, Wideband HF Technology, has shown that an adaptive inverse filter can be designed for the HF channel to achieve bandwidths up to 1 MHz (reference 5)**. Project 7140 implemented an all-digital adaptive filter using medium-scale and large-scale integration (MSI and LSI) transistor-transistor-logic (TTL), high-speed analog-to-digital converters (ADC), and digital-to-analog converters (DAC). The function of the all-digital filter can be performed by several PTF Modules with the benefits of at least an order-of-magnitude reduction in size and two orders-of-magnitude reduction in power consumption.

The inverse filter used for equalization compensates for both amplitude and phase distortions introduced by the channel. Therefore a CCD-based equalizer is realized at baseband similar to the digital equalizer already constructed. The receiver signal is

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* Section 2.4 briefly discussed device performance.

** Normal HF channels are restricted to approximately 10 kHz of coherent bandwidth.

first down-converted to baseband by two local oscillators and then processed by in-phase and quadrature (or real and imaginary channels). The signal s(t) is processed by this complex filter, whose impulse response is h(t). The output, y(t), is given by

$$y(t) = s(t)*h(t). \tag{1}$$

where * denotes the linear convolution operation. The output can also be written as

$$y(t) = [s_R(t) + js_I(t)] * [h_R(t) + jh_I(t)] \tag{2}$$

where the R and I subscripts designate the real and imaginary components of the signal and the filter impulse response. The function y(t) can be rewritten as

$$y(t) = y_R(t) + jy_I(t) \tag{3}$$

where

$$y_R(t) = s_R(t)*h_R(t) - s_I(t)*h_I(t) \tag{4}$$

and

$$y_I(t) = s_R(t)*h_I(t) + s_I(t)*h_R(t) \tag{5}$$

To realize a complex filter, four convolutions must be performed. The convolutions require four transversal filters. Figure 10 shows the configuration of the baseband equalizer.

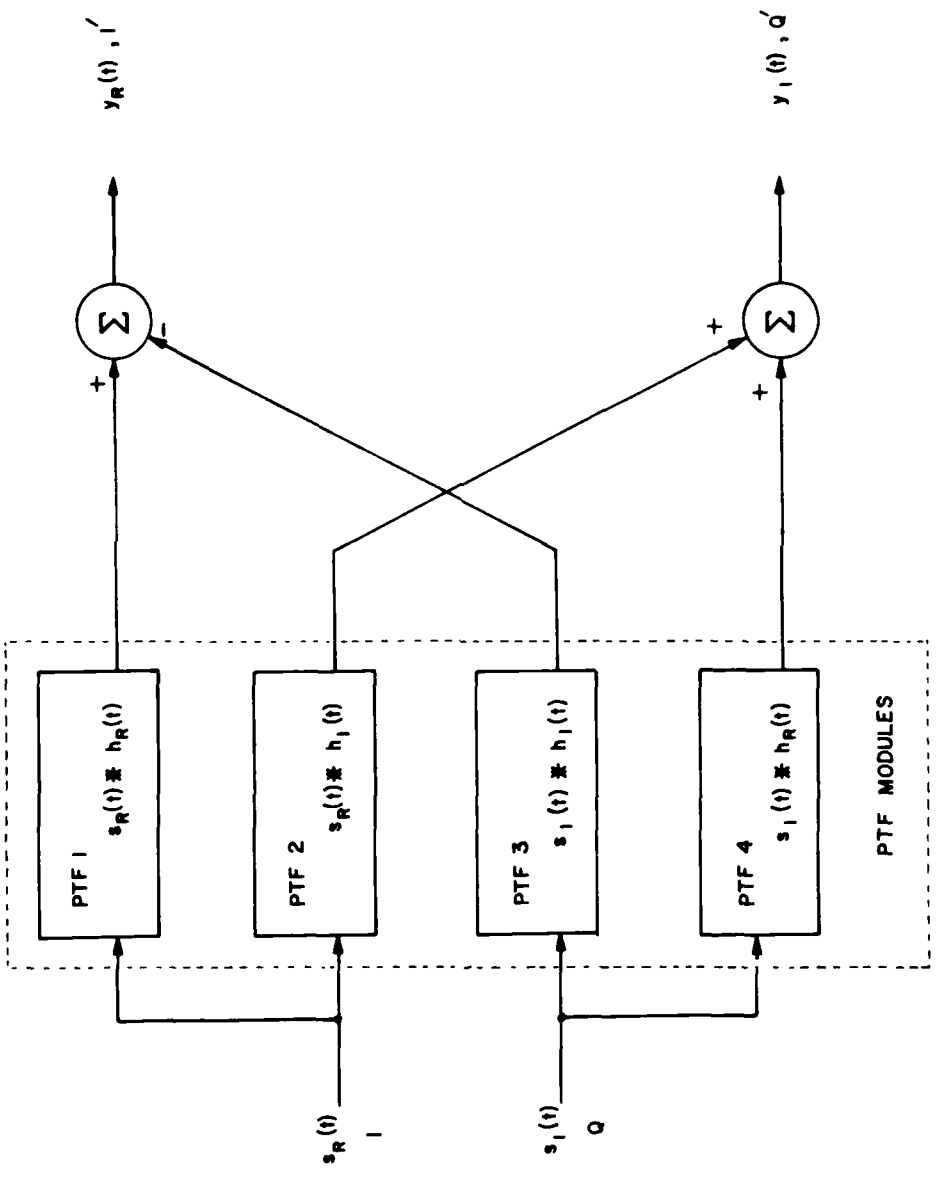

Figure 10. Adaptive Equalizer

The impulse response and its real and imaginary components are derived from the inverse Fourier transform of the amplitude and phase characteristics of the channel which are obtained by sine wave testing of the channel. There are 128 tap weight coefficients for each transversal filter. The coefficients, calculated by a minicomputer, are 8 bits in length. The filter length and coefficient word length are ideally matched to the PTF.

The CCD-based adaptive equalizer and its performance will be compared to the all digital filter now used in the Adaptive HF System. This evaluation will be performed in the test bed shown in figure 11. The test bed consists of an HP 2115 minicomputer, flexible-disk storage system, CRT terminal, high-speed digital word generator, high speed buffer memory, several ADCs and DACs and the CCD equalizer under test. The minicomputer is used primarily as a controller but can be used to calculate the tap weights of the adaptive filter. Normally, the filter coefficients are calculated on a larger compatible computing facility. The flexible disk-storage system is used to read data files which contain a stored version of a known signal transmitted over the HF channel. These recordings were obtained on Project 7140's HF System. The disk storage is also used to record the results of the equalized signal. The high-speed word generator is required to provide real-time replication of the transmitted signal. The input/output capability of the minicomputer is too slow to handle this task. A block of digital data, read from the flexible disk, is loaded into the word generator and then read out at the desired rate. The outputs of the word generator drive two DACs that recreate the I and Q analog signals. The signals are processed by the CCD equalizer and the outputs of the equalizer, I' and Q', are converted back to digital form for storage. The input channel of a high-speed buffer memory is used to receive the digitized version of the equalized

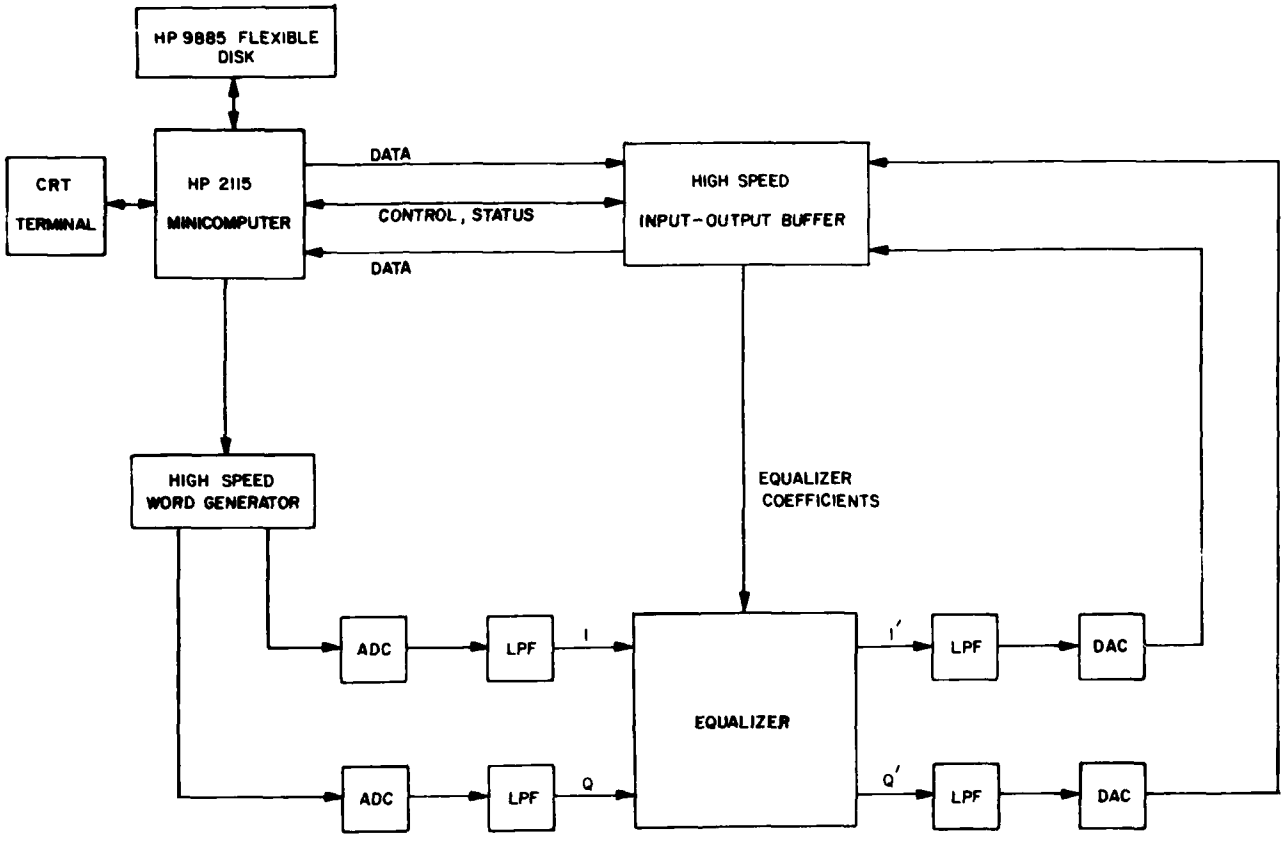

Figure 11. Computer-Controlled Adaptive Equalizer Test Configuration

signal at a real-time rate. The contents of the buffer memory are periodically loaded onto the flexible disk for permanent storage and later evaluation. The output channel of the same buffer memory is used to store and load the filter coefficients of the calculated inverse filter into the four PTF Modules used in the equalizer.

The test bed described will enable us to evaluate the performance of a CCD transversal equalizer for HF channel equalization. When completed, the test bed will also be used for general programming and evaluation of the PTF Modules.

4.3 SPREAD-SPECTRUM MODEM

Another important system application for the PTF Modules being explored by Project 7170 is spread-spectrum communications. The PTF Modules form the kernel of a spread-spectrum modem being developed for a wideband HF channel. The modem utilizes direct pseudo-noise (PN) phase coding of the transmitted digital data to spread the signal bandwidth and suppress jamming and interference. The PTF Modules are used as matched filters for the phase-coded signal. These matched filters provide pulse compression and increase the peak signal to rms noise of the desired signal over the jamming signal to improve detection. A schematic of the modulator and demodulator used in the spread-spectrum system is shown in figure 12.

The modem uses binary phase-shift-keying (BPSK) coding of the transmitted data bit for spreading the modulation. The modem also has differential binary and quadrature PSK data modulation capability. Differential phase modulation removes the $\pm 180^{\circ}$ phase ambiguity at the receiver. The data to be transmitted is encoded as

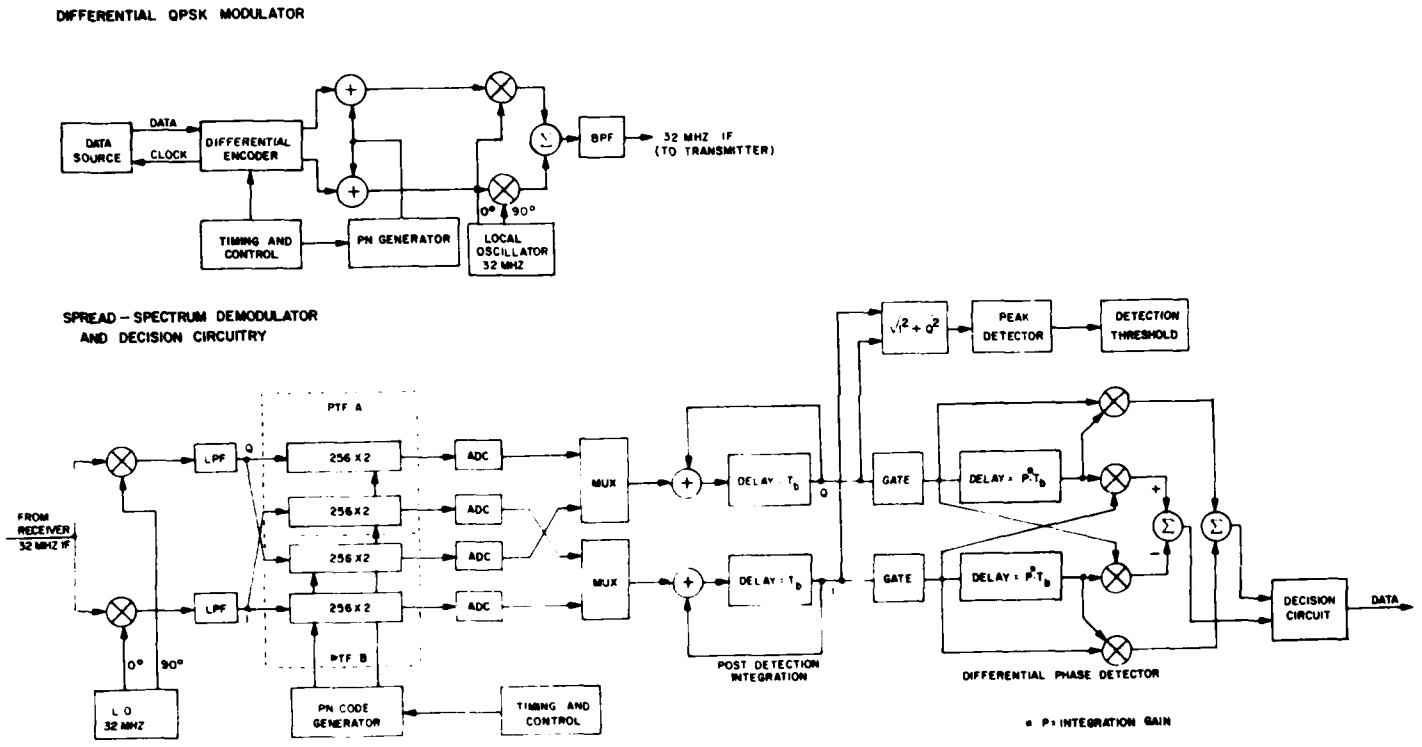

Figure 12. Spread Spectrum Modem

the phase of the transmitted signal. Differential PSK modulation uses the phase comparison of two successive received vectors to determine the data transmitted. This requires preservation of the received-vector phase. Therefore, differentially coherent operation necessitates that the demodulator have both in-phase (I) and quadrature (Q) channels to operate successfully. The outputs from the I and Q channels are orthogonal components of the received vector. The differential phase is extracted from the two successive sets of orthogonal components (i_1, q_1) and (i_2, q_2) received.

The spread spectrum matched filters used by the demodulator are realized by two PTF Modules, each configured in the dual 256 x 2-bit mode. The specified system requires continuous data transmission capability and also requires that different PN codes be overlaid on each successive data bit. The different matched filters required for each coded bit are realized by reprogramming the PTF. Two modules are used because the PTF Module cannot process signals while it is being reprogrammed. Therefore, two modules, each with a 50% duty cycle, are multiplexed to provide continuous processing of the serial data. The dual 256 x 2-bit mode was selected for each module so that the matched filters for the I and Q channels, which are programmed with the same code, are in the same modules. The 256 x 2 mode provides a 24 dB processing gain improvement. The two bit mode must be used to realize the +1 and -1 weighting coefficients of the binary phase code.

The modem has the following preliminary specifications:

Equivalent Noise Spreading Bandwidth			B_{ss}	= 512 kHz
PN Chip Duration	T_c	=	$1/B_{ss}$	= 1.95 μs
Data Symbol Duration	T_d	=	NT_c	= 500 μs
Symbol Bandwidth	B_d	=	$1/T_d$	= 2 kHz
Maximum Data Rate				
BPSK			R_{DB}	= 2 kHz
QPSK			R_{DQ}	= 4 kHz

The spread spectrum processing gain, defined as (B_{ss}/B_d), is desired to be a minimum of 24 dB which is provided by the PTF matched filters. Additional processing gain of up to 6 dB is obtained by post detection integration. This integration gain is realized at the expense of the data rate.

The use of the PTF Modules as programmable matched filters in spread spectrum communications provides an important signal processing capability for military communications. A more detailed description of the modem's implementation and the results of its experimental evaluation will be provided separately.

REFERENCES

1. Roger A. Haken, Robert C. Pettengill, and Larry R. Rite, "A General Purpose 1024-Stage Electronically Programmable Transversal Filter," IEEE Journal of Solid State Circuits, December 1980.

2. Roger A. Haken and Robert C. Pettengill (Texas Instruments, Inc.), "Binary/Analog CCD Correlator Development," RADC-TR-79-211 Interim Report, Rome Air Development Center, September 1979, ADA077572.

3. A. V. Oppenheim and R. W. Shafer, Digital Signal Processing, Englewood Cliffs, W. J.: Prentice-Hall, 1975.

4. M. J. Howes and D. V. Morgan, ed., Charge Coupled Devices and Systems, New York: John Wiley and Sons, 1979.

5. Bernard D. Perry, "Design and Implementation of Project 7140 Wideband HF Communication Test Facility," The MITRE Corporation, Bedford, MA, September 1980, ESD-TR-81-135, July 1981, ADA102261.

APPENDIX A

TEST BED CIRCUIT DESCRIPTION

The PTF Test Bed consists of a combination of analog and digital circuits which can be classified in the three general categories of power, control/data, and signal circuitry. The following detailed discussion of circuit operation combines both the PTF Module and PTF Exerciser Module to unify the test bed description.

A.1 POWER

The PTF Test Bed derives its prime power from several external power supplies. Various voltages are routed via the modified back-plane of a Tektronix TM506 Power Module. The PTF Module is provided with $\pm$ 15 VDC for its analog circuitry and +5 and +15 VDC for its digital circuitry from two Tektronix power supplies (PS503, PS501/1) via the modified back-plane, as shown in figure A-1.* To allow for bias adjustment, the PTF module contains several adjustable voltage-divider networks to set the PTF device DC bias voltage levels. Typical values for the bias voltages are shown in table A-1.

The PTF Exerciser Module has three internal power supply circuits which are driven by voltages supplied by the TM506. The power supply circuits and their input and output voltages are shown in figure A-2.

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* Separate power supplies are used for the analog and digital circuitry in the PTF device to minimize the effects of noise.

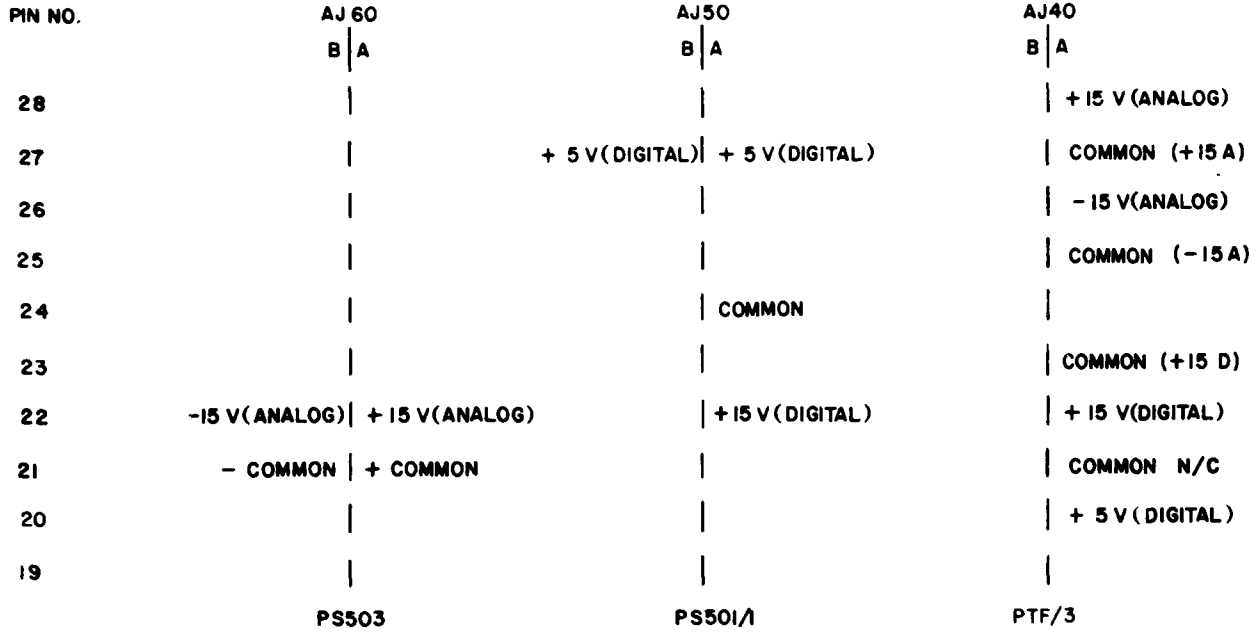


Figure A-1. Modified Section of TM506 Back-Plane

Table A-1

PTF 2/3 Bias Voltages

Bias Voltage	Level	Function
V_{SUB}	-5 V	Sets a suitable back bias substrate Voltage to enhance the operation of the NMOS device.
V_{FZ}	12 V	Establishes the fixed level of background charge in each CCD energy well necessary to reduce charge transfer inefficiency caused by surface states and permits inputting bipolar signals.
V_{REF} (1)	7.5 V	Sets DC bias point for PTF output amplifiers and charge amplifiers.
V_{REF} (2)	5.8 V	Sets DC bias point for input amplifiers.
ϕ_3	2 V	Gate DC bias voltage for ϕ_3 transfer electrode.
ϕ_2"	12 V	Gate DC bias voltage for ϕ_2" transfer electrode.

Note: These biases are adjustable off-chip to evaluate their effect on device performance. Production chips would be expected to have fixed bias set by on-chip circuitry.

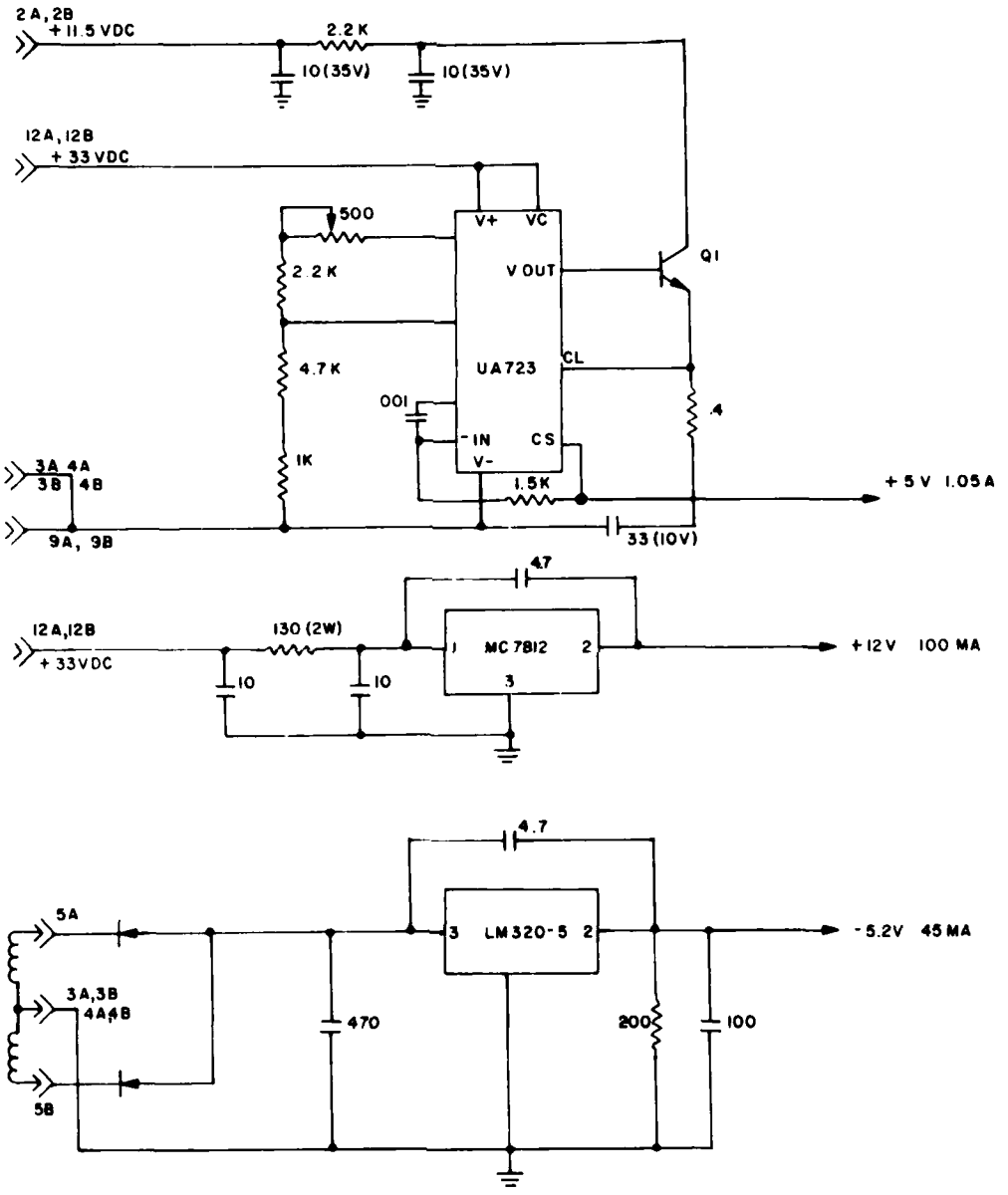


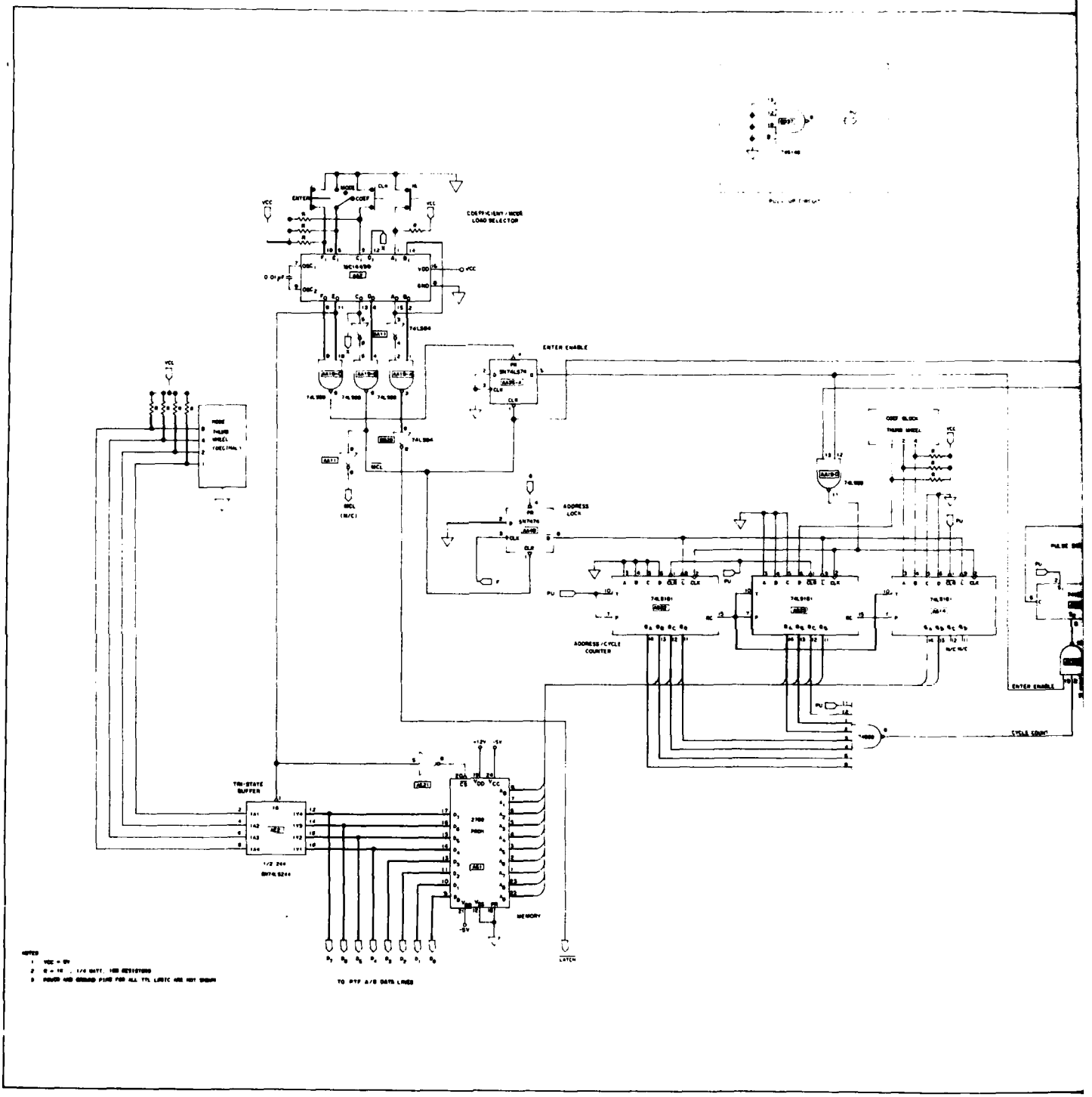
Figure A-2. PTF Exerciser Module Power Supplies

A.2 CONTROL/DATA

Digital circuits, primarily in the PTF Exerciser Module (figures A-3 and A-4), perform the operations of system timing, PTF synchronization, mode load, and coefficient programming. The Control/Data signals are routed between the PTF Exerciser Module and PTF Module via cable made up of 18 twisted wire pairs. The connections of these twisted pairs are shown in figure A-5. Each twisted pair is terminated with a 220Ω pull-up resistor and a 330Ω pull-down resistor to match the 132Ω characteristic impedance of the twisted pair.

A.2.1 System Timing

The master clock (MC) is generated by a standard pulse generator and input to the PTF Exerciser Module via a front panel BNC connector. This clock signal, which is terminated with 50Ω , is routed into a flip flop which is used to reduce the MC frequency (f_{mc}) by a factor of two. The divide-by-two flip flop output signal, termed System Clock One (SC/1), is used to drive the 4-phase CCD at the basic CCD cycle rate of f_c, where f_c is one-fourth the rate of the SC/1 clock input. The divide-by-two flip flop also creates the required 50% duty cycle of SC/1. SC/1 is also routed into the PTF Synchronizer circuit and into a synchronous 4-bit counter configured to further reduce the SC/1 frequency by the factor N+1 where N ranges from 0 to 9 and is selected by a thumbwheel on the front panel of the PTF Exerciser Module. The output of the counter is an asymmetrical clock (SC/2) which is directed to the input of a pulse synchronizer.


COEFFICIENT / MODE LOAD SELECTOR
ENTER ENABLE
ADDRESS LOCK
ADDRESS / CYCLE COUNTER
TRI-STATE BUFFER
MEMORY
TO PTF A/B DATA LINES
LATCH

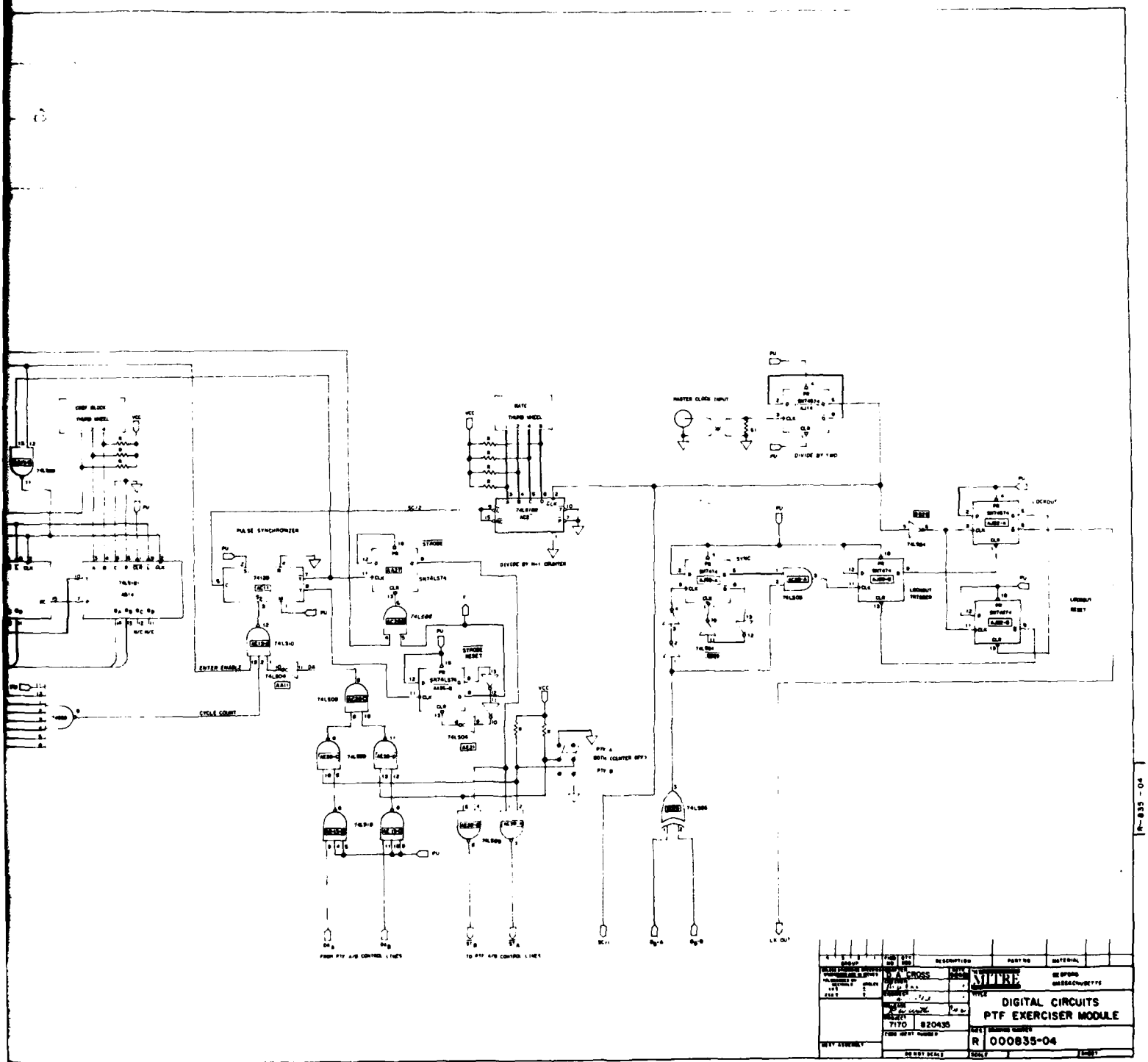


Figure A-3. PTF Exerciser Module: Digital Circuits

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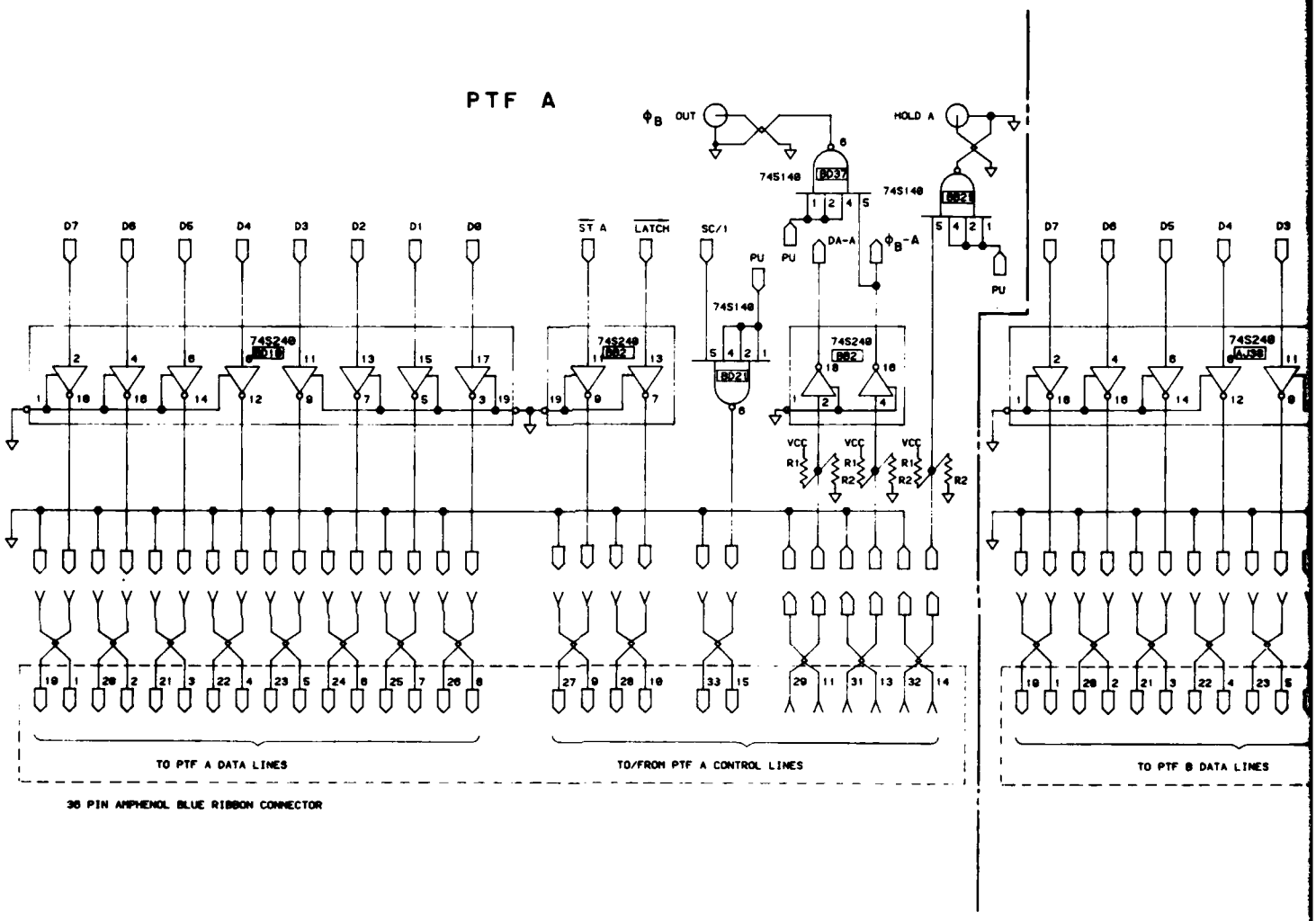
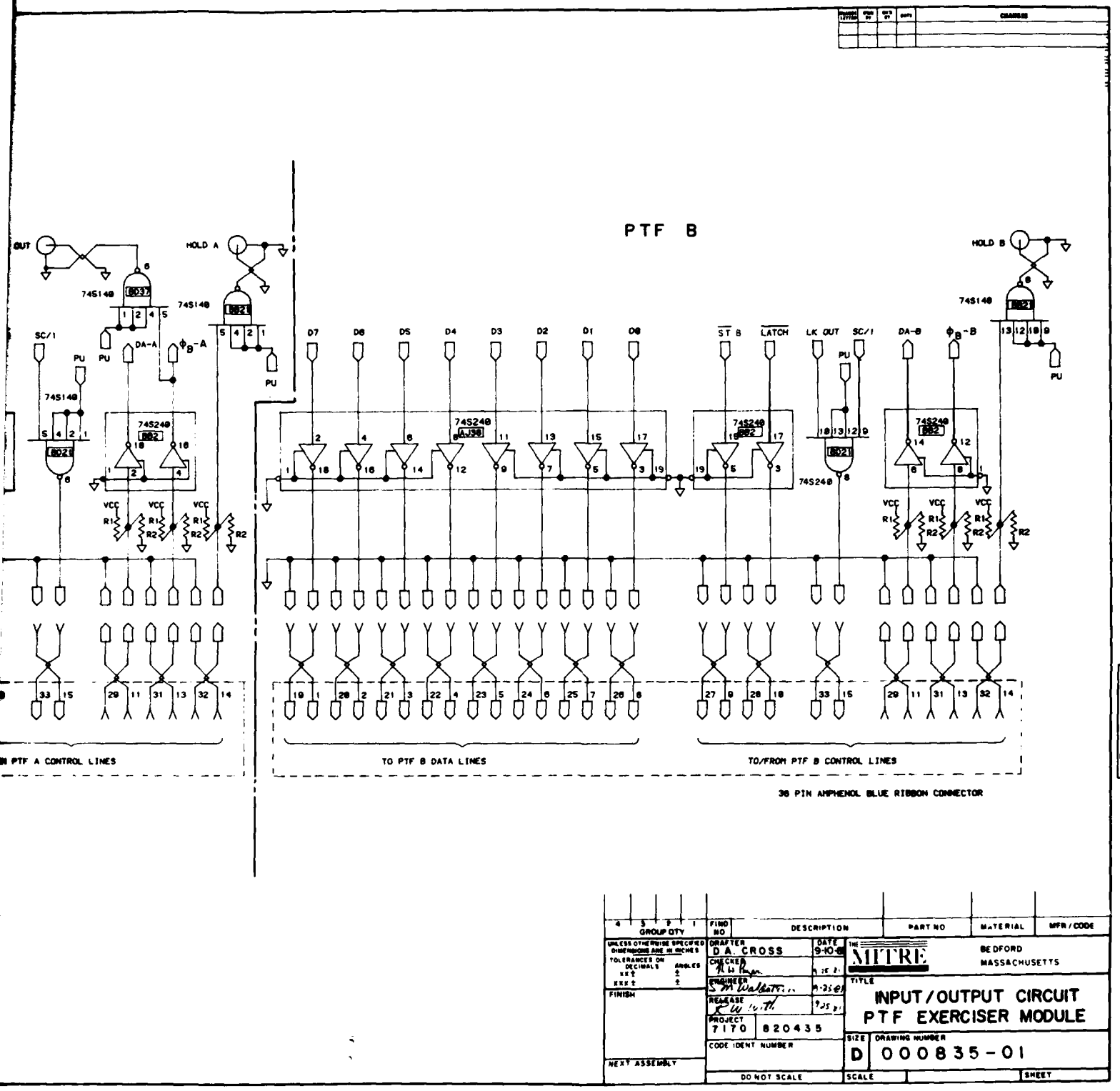


NOTE

1. ALL R1 AND R2 RESISTORS ARE IN A SINGLE IN-LINE PACKAGE (SIP), BECKMAN PART NO. 787-S-R220/330.

   ALL PULL-UP RESISTORS SHARE A COMMON VCC AND ALL PULL-DOWN RESISTORS SHARE A COMMON GROUND.

   R1 = 220Ω AND R2 = 330Ω.



DRAFTER	D.A. CROSS	DATE	9-10-81
CHECKED			
ENGINEER	S.M. Walker		9-25-81
RELEASE			9-25-81
PROJECT	7170 820435		
CODE IDENT NUMBER			
NEXT ASSEMBLY			

THE MITRE — BEDFORD MASSACHUSETTS

TITLE: INPUT/OUTPUT CIRCUIT PTF EXERCISER MODULE

SIZE D — DRAWING NUMBER 000835-01

DO NOT SCALE — SCALE — SHEET

D-83501

Figure A-4. PTF Exerciser Module: Input/Output Circuits

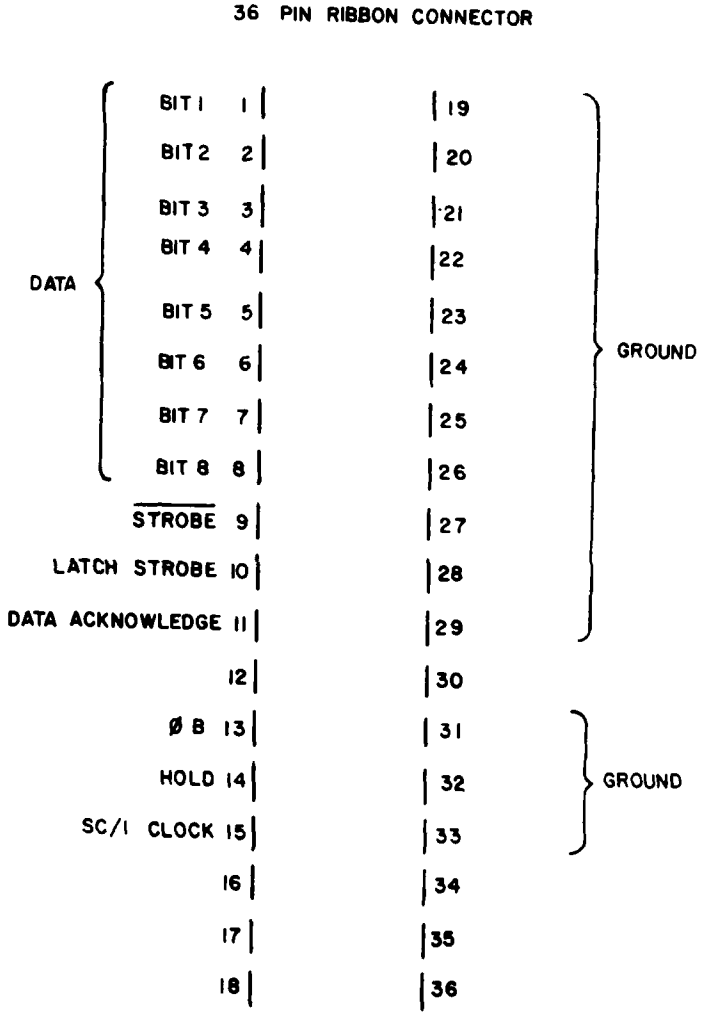


Figure A-5. Cable Diagram for Digital I/O Port

A.2.2 PTF Synchronizer

The PTF Synchronizer circuit synchronizes the operation of two PTFs for applications requiring longer filter lengths, greater coefficient accuracy, or parallel filtering. This synchronization is accomplished by aligning the $\emptyset_B$ clock of any two or more PTF modules. The $\emptyset_B$ clock, which is generated internal to the TI PTF chip, is the clock used to sample the analog input signal. The circuit that performs the synchronization is shown in figure A-3 (also A-6). The $\emptyset_B$ outputs of two PTFs are inverted and input to an exclusive-or gate (BD29). This gate generates an output pulse whenever one PTF A or PTF B $\emptyset_B$ pulse occurs noncoincidentally with the other. When the $\emptyset_B$ signals are in synchronization, the Lockout flip flop is in a steady-state condition with its CL line low and Q high. The Lockout flip flop Q is input to a NAND gate (BD21 on figure A-4) along with SC/1. The NAND gate output provides the system clock signal for PTF B. As long as the devices are in synchronization, Q remains high and the NAND gate output changes with the SC/1 input. As a result, PTF B is clocked at the same rate as PTF A. In the event the PTFs are out of synchronization, the SYNC flip flop clock input will go high whenever one PTF $\emptyset_B$ occurs but not the other. This will cause the SYNC flip flop to generate a short pulse at its Q output. This pulse will occur within the period of the SYNC CLOCK pulse, as shown in the timing diagram of figure A-6, but delayed a finite time from the SYNC CLOCK pulse's rising edge. The SYNC CLOCK and SYNC Q pulses are input to an AND gate which, by virtue of the SYNC Q pulse delay, prevents glitches from clocking the Lockout Trigger flip flop. Only a valid SYNC Q pulse can cause the Lockout Trigger flip flop to be clocked. When the Lockout Trigger flip flop is clocked, its Q output goes high, setting the Lockout flip flop CL high. On the next negative going edge of the SC/1 clock, the Q of the Lockout flip flop is driven

low. NANDing this signal with the SC/1 clock prevents PTF B from being clocked by the next SC/1 pulse. On the following negative going SC/1 pulse, the Lockout Reset flip flop resets the Lockout Trigger flip flop so that it is ready to respond to another SYNC CLOCK pulse. This action also puts the Lockout flip flop CL low, returning its Q high and therefore allowing the PTF B correlator to be clocked. If the correlators are now in sync, the circuitry remains in steady state. If the correlators are out of sync, the previous cycle (withholding the PTF B clock for one cycle while the PTF A clock continues to operate) repeats until the $\emptyset_B$ signals are synchronized.

A.2.3 Mode Load

The mode load circuitry generates the signals required to set up any one of the nine PTF modes. Placing the Coefficient/Mode Select switch on the front panel of the PTF Exerciser Module in the Mode position causes the tri-state buffer (figure A-3) to route the output of the decimal Mode Thumbwheel to PTF data lines A through D (in the PTF Module) via line drivers and receivers. The tri-state buffer reduces the number of wires and the size of the connector required between the PTF Exerciser and PTF Module by allowing four of the connecting data lines to be shared by the mode and coefficient signals. To latch the mode into the PTF the latch push-button is depressed, creating a latch strobe signal which flows to the latch input on the PTF. Data on the mode input lines will only be allowed to enter the device during the period of the latch strobe pulse.

A.2.4 Coefficient Load

To initiate a coefficient load operation the Coefficient/Mode Select switch is placed in the COEF position (figure A-3). This enables the memory and the tri-state buffer so that coefficients are

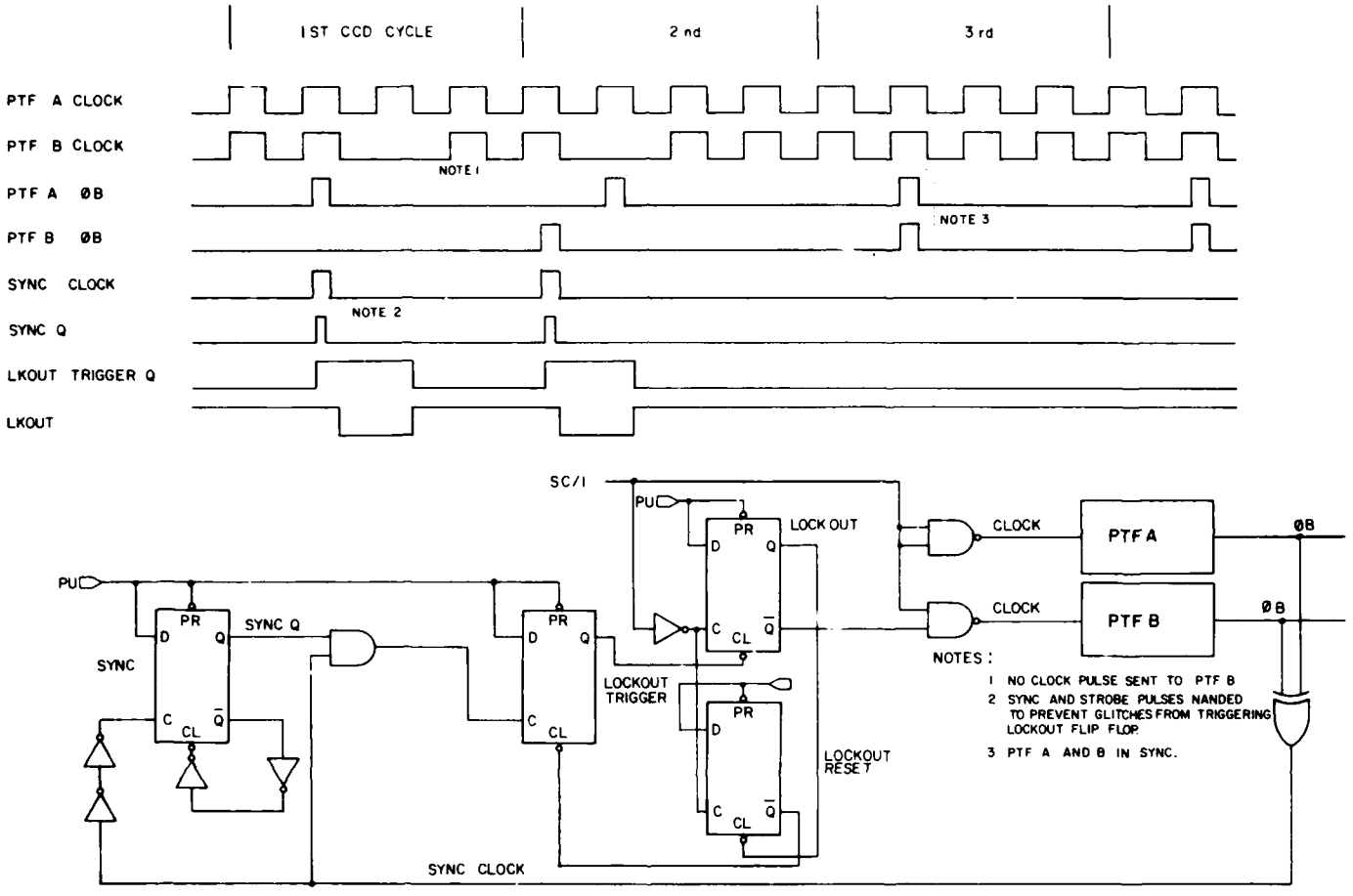


Figure A-6. PTF Synchronizer

directed to the output data lines D_0 through D_7. Next, depressing the CLR button drives the MCL line low which sets up the proper initial conditions to generate a pulse by the Enter Enable flip flop and the correct starting address of the Address/Cycle Counter. The COEF BLOCK Thumbwheel is operated to select the desired block of 128 8-bit words in memory where the filter weighting coefficients are stored. The decimal output of the thumbwheel is routed to the three most significant bits of the input lines of the 10-bit counter. Depressing the ENTER push-button commences the coefficient enter cycle by causing the output of the Enter Enable flip flop to go high. This ENTER ENABLE signal is routed to a NAND gate (AA19) where it enables the Address/Cycle Counter to be clocked. It is also NANDed with two other signals on the S_2 input to the Pulse Synchronizer. The Pulse Synchronizer is configured to pass a single input pulse to its output under the control of three signals from other circuit elements. These control signals are the DA output from the PTF/3 microprocessor interface circuitry, the coefficient load cycle counter output from the 10-bit Address/Cycle Counter and the ENTER ENABLE signal, generated by depressing the front panel ENTER button. With these three control signals high, i.e., at the initiation of a load sequence, their NANDed input (low) to the Pulse Synchronizer S_2 control line results in a single Synchronizer output pulse in sync with the SC/2 clock. The $\overline{Q}$ output pulse clocks the $\overline{\text{STROBE}}$ flip flop, and the Address/Cycle Counter, while the Q output pulse clocks the $\overline{\text{STROBE}}$ Reset flip flop. The $\overline{\text{STROBE}}$ flip flop and $\overline{\text{STROBE}}$ Reset flip flop are configured to generate an asynchronous $\overline{\text{ST}}$ pulse when clocked by the Pulse Synchronizer. The $\overline{\text{ST}}$ pulse is routed to the PTF microprocessor interface circuitry (internal to the PTF) which responds by driving its Data Acknowledge (DA) output line high until the PTF loads the addressed coefficient. This signal causes the S_2 input line of the Pulse Synchronizer to go high, ensuring that no further asynchronous $\overline{\text{ST}}$ pulses are generated

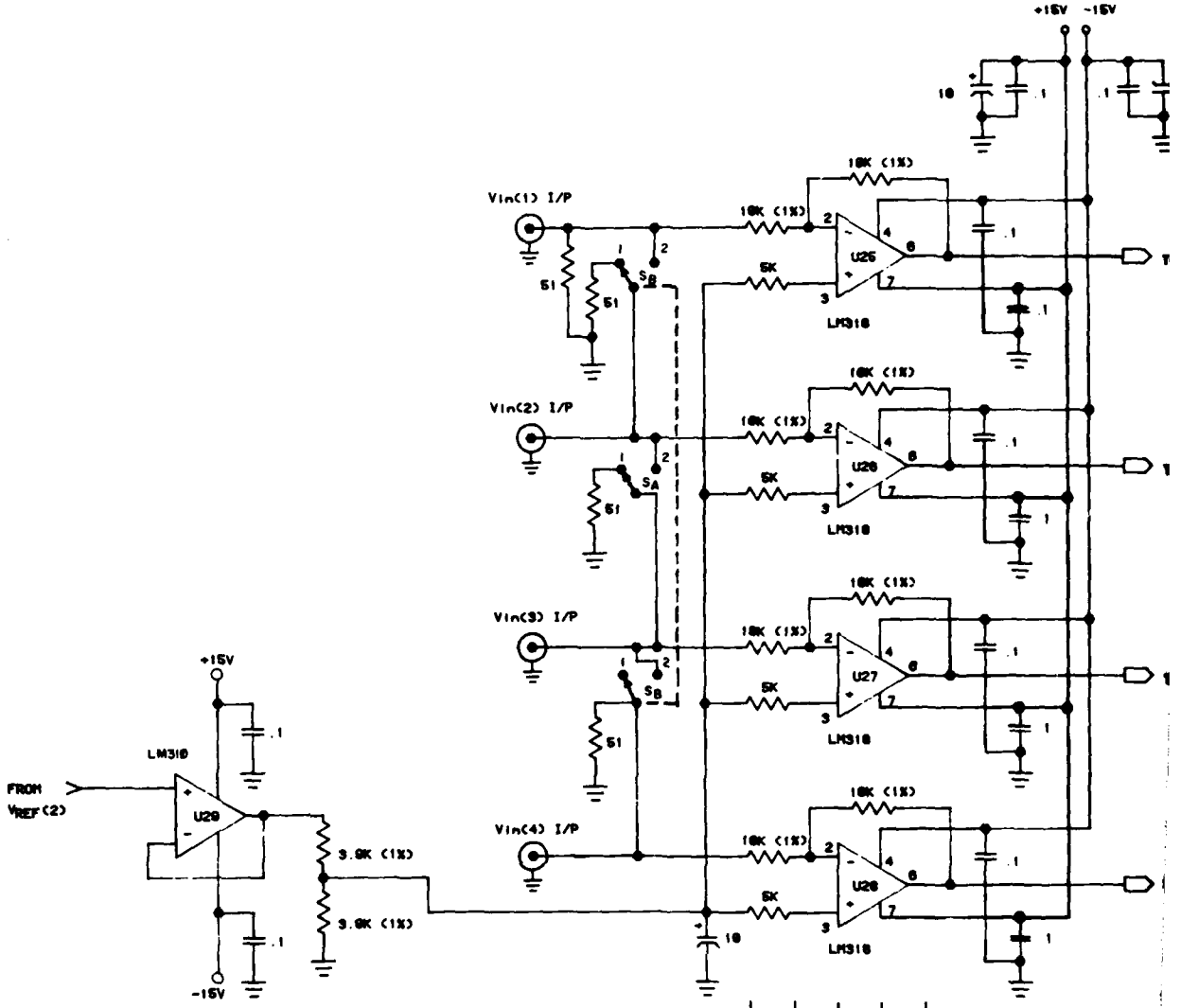
until the PTF device has loaded the addressed 8-bit coefficient word.

The first $\overline{\text{STROBE}}$ Reset flip flop output pulse of the coefficient load cycle also serves to lock the output of the COEF BLOCK Thumbwheel into the Address/Cycle Counter by clocking the Address Lock flip flop. Subsequent pulses at the Pulse Synchronizer Q output clock the Address/Cycle Counter to the remaining 8-bit coefficient words in memory.

When the PTF device completes the loading of an 8-bit coefficient word, the DA line returns to its low state. This permits the Pulse Synchronizer to pass another SC/2 clock pulse. The 8-bit coefficient word cycle repeats until all 128 coefficient words have been programmed into the PTF. The cycle is stopped when the output of the counter NAND gate (AC37) goes low on the 127th count. This output is one of the three control signals to the Pulse Synchronizer; a low signal stops the Pulse Synchronizer from passing SC/2 pulses to the output. At the completion of the coefficient programming the PTF is configured to process analog input signals.

A.3 SIGNAL

All analog signal conditioning circuitry is located inside the PTF Module (figures A-7, A-8 and A-9). Four input connectors for $V_{in}(1)$, $V_{in}(2)$, $V_{in}(3)$, and $V_{in}(4)$ are located on the front panel of the PTF Module. These signals are routed into the input switching circuit which directs the signals to be filtered into the appropriate PTF device input pins for the selected mode of operation. Table B-1 shows the required switch positions for the several PTF modes. Unity gain amplifiers buffer the input and provide the DC offset of a bipolar signal required by the PTF. The



NOTES:

1. ALL CAPACITORS ARE IN MICROFARAD UNLESS SPECIFIED.
2. ALL RESISTORS ARE IN OHMS UNLESS SPECIFIED.

4	3	2	1	GROUP QTY	FIND NO.	DESCRIPTION

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ON DECIMALS .xx ± .xxx ± ANGLES ±

FINISH

NEXT ASSEMBLY

DRAFTER	D. A. CROSS	DATE 9-8-
CHECKER	A. W. Pagon	9-25-
ENGINEER	K. Waldstein	9-25
RELEASE	R. W. Wirth	9-25
PROJECT	7170	820435
CODE IDENT. NUMBER		

DO NOT SCALE

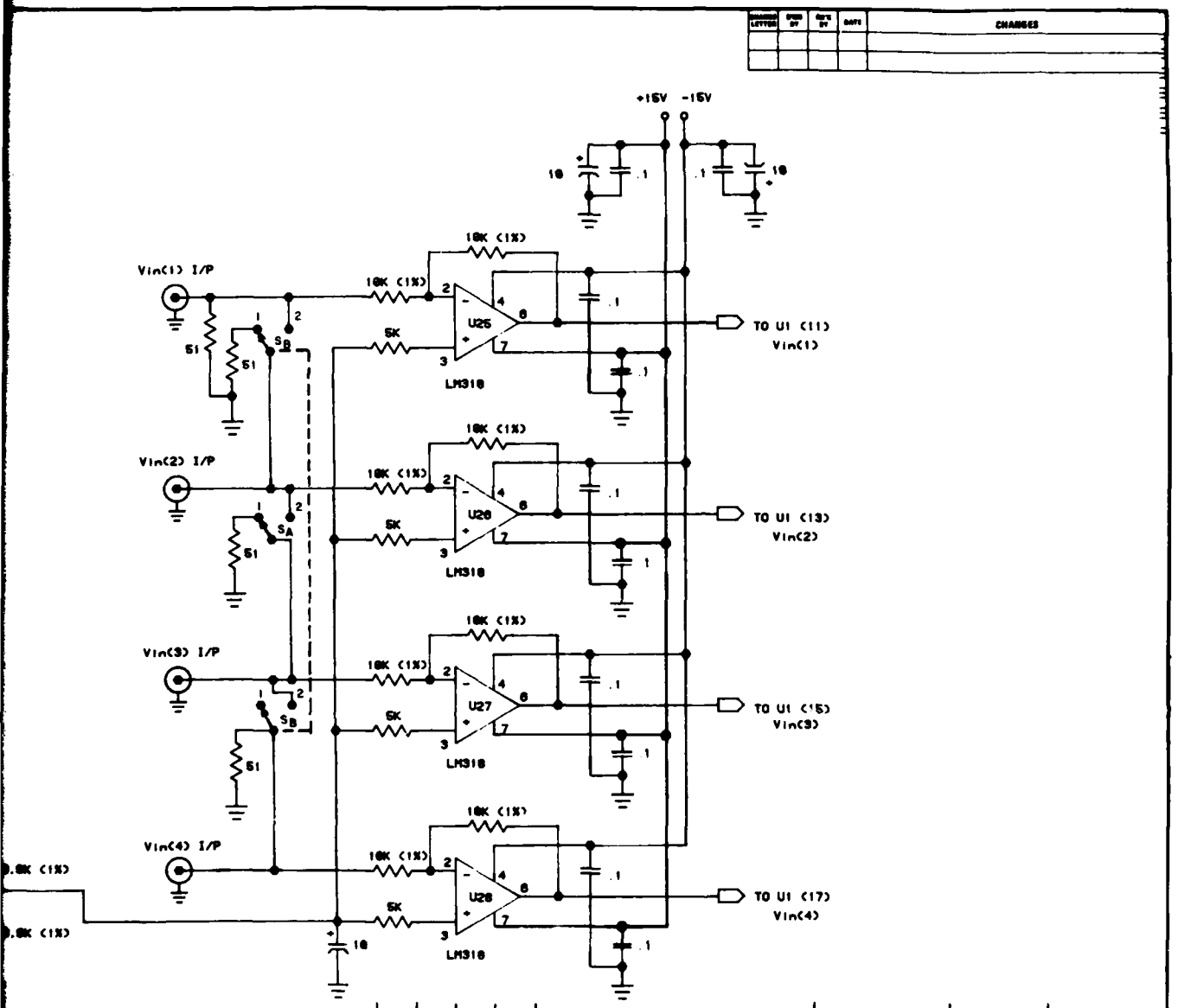
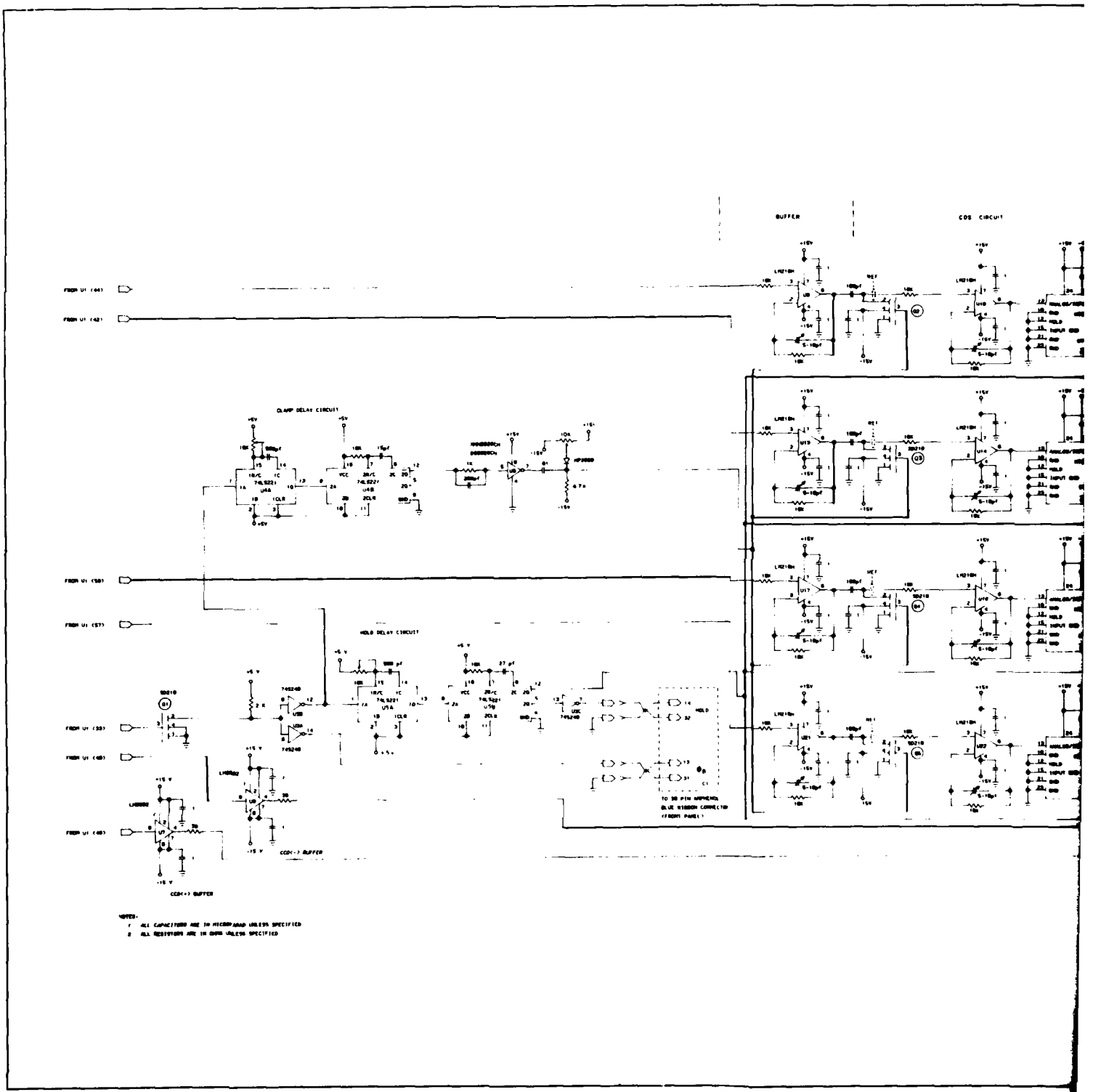


Figure A-7. PTF Module: Input Circuits


BUFFER
CDS CIRCUIT
CLAMP DELAY CIRCUIT
HOLD DELAY CIRCUIT
CCD(-) BUFFER
CCD(+) BUFFER
TO 36 PIN AMPHENOL
BLUE RIBBON CONNECTOR
(REAR PANEL)

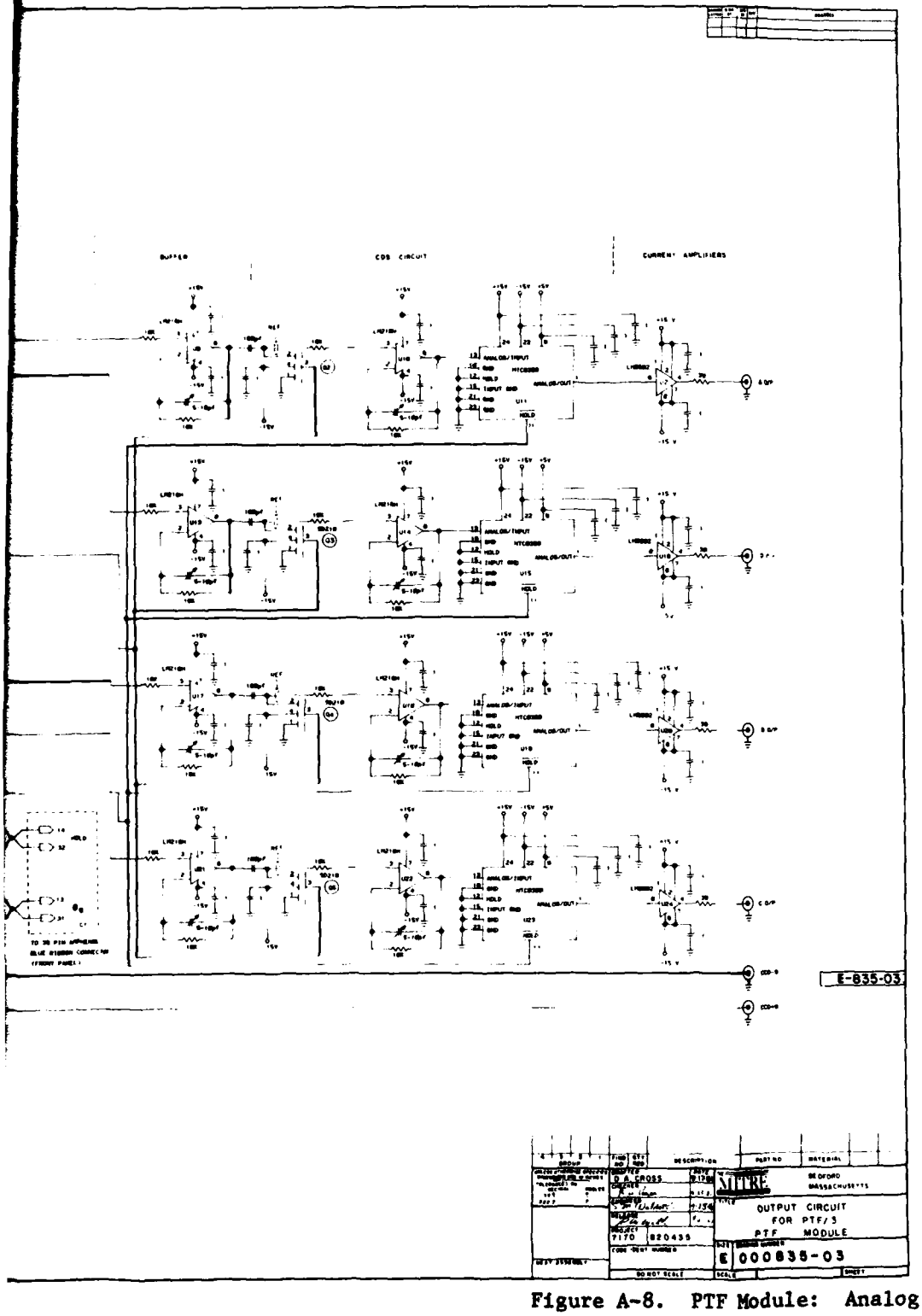


Figure A-8. PTF Module: Analog Output Circuits

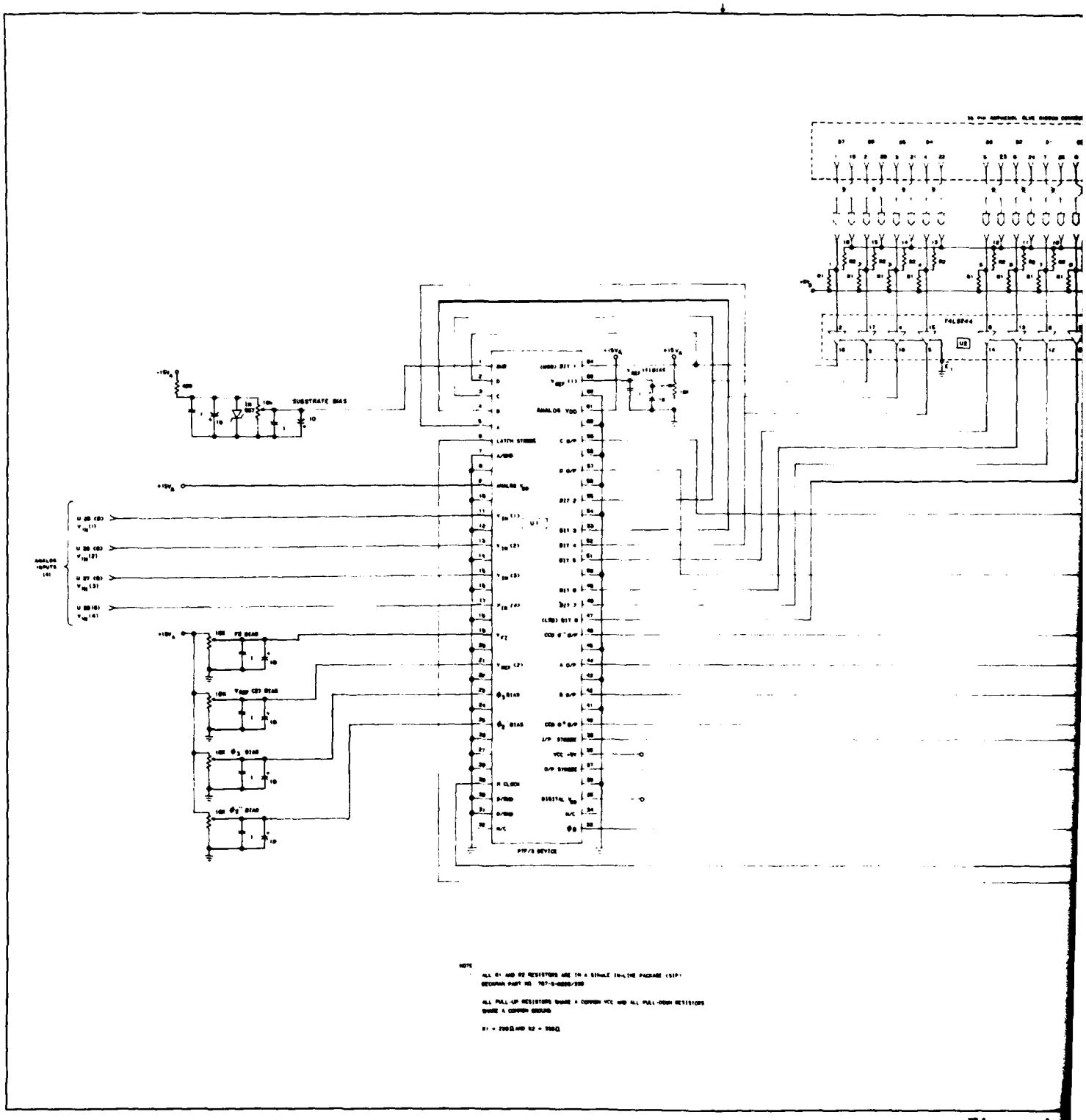


Figure A-

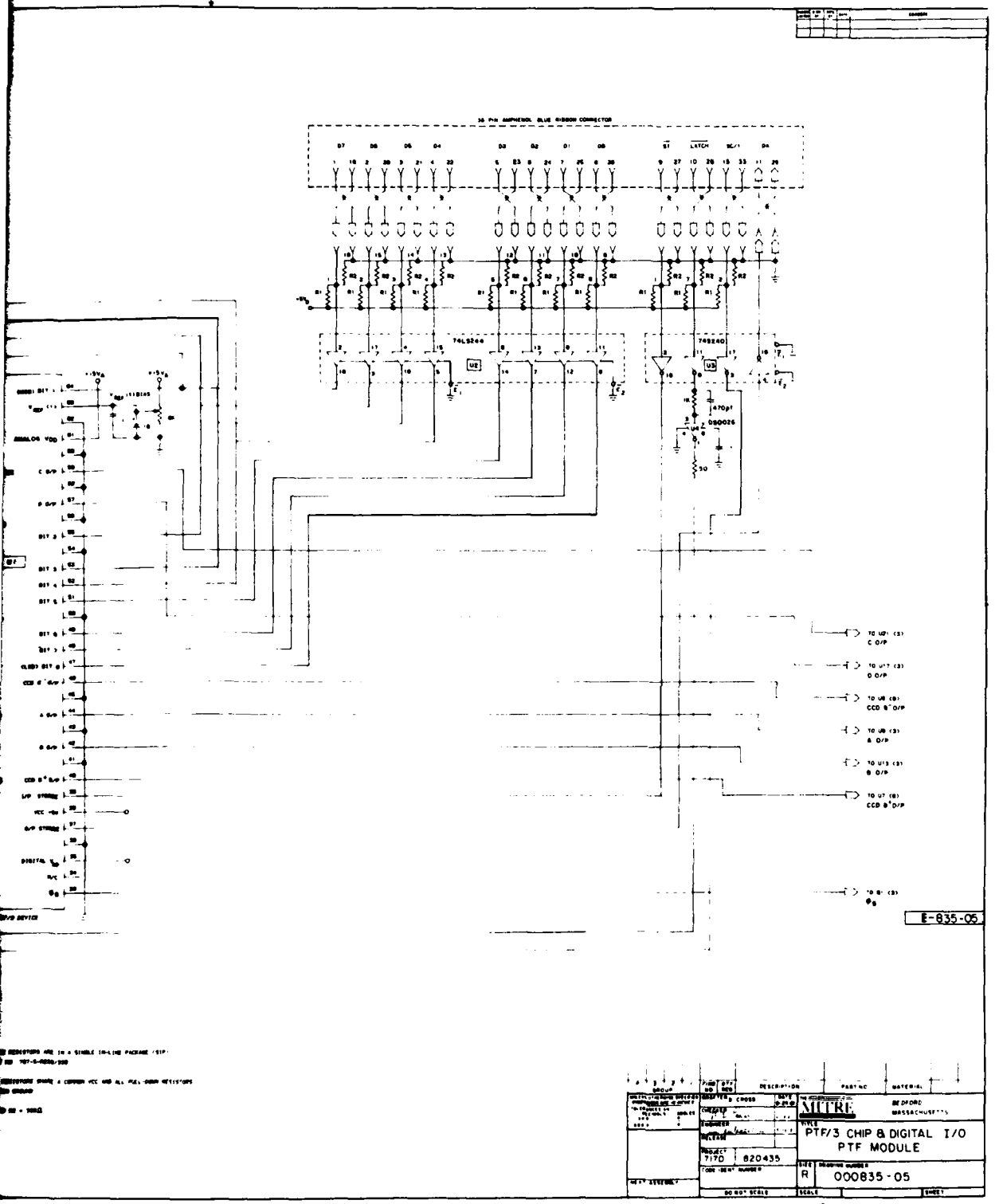


Figure A-9. PTF Module: PTF/3 Chip and Digital I/O Circuits

input signal exits the PTF, after the filtering operation, and is routed into the Correlated Double Sampler (CDS) circuit. The output of the PTF for a single CCD cycle is illustrated in figure A-10. Just after the CCD reset period the CCD output is preset to a DC reference voltage. This DC level must be removed to recover the CCD filtered analog signal. The voltage at the Reference point (REF), shown in figure A-8 is clamped to V_{REF} between the CCD reset period and the CCD integration period. Between these two periods, a FET switch (Q27 for the A O/P) is closed and then opened by a CLAMP pulse. This action combined with the high input impedance of the subsequent impedance buffer results in the V_{REF} charge being isolated at the REF point. Subsequently, as the CCD output voltage rises to the V_s level, the voltage at REF is the difference between V_s and V_{REF}. When the CCD has completed integrating charge, the track and hold (T/H) circuit samples the signal during the HOLD pulse. The T/H output is then the desired filtered analog signal. The filtered signal is next routed into a current amplifier which interfaces it with external equipment.

The CLAMP and HOLD pulses are generated by the delay circuits which use the $\emptyset_B$ clock as the reference timing signal. The $\emptyset_B$ signal is routed into a FET transistor (Q1), which converts the PTF $\emptyset_B$ signal level to TTL, and then into multivibrators (U4 and U5). The multivibrators are configured to provide the necessary delay so that the CLAMP and HOLD pulses occur during the appropriate CCD intervals shown in figure A-10. After the clamp signal has been generated, a TTL-to-MOS converter (U6) is used to drive the gate of the FET switch.

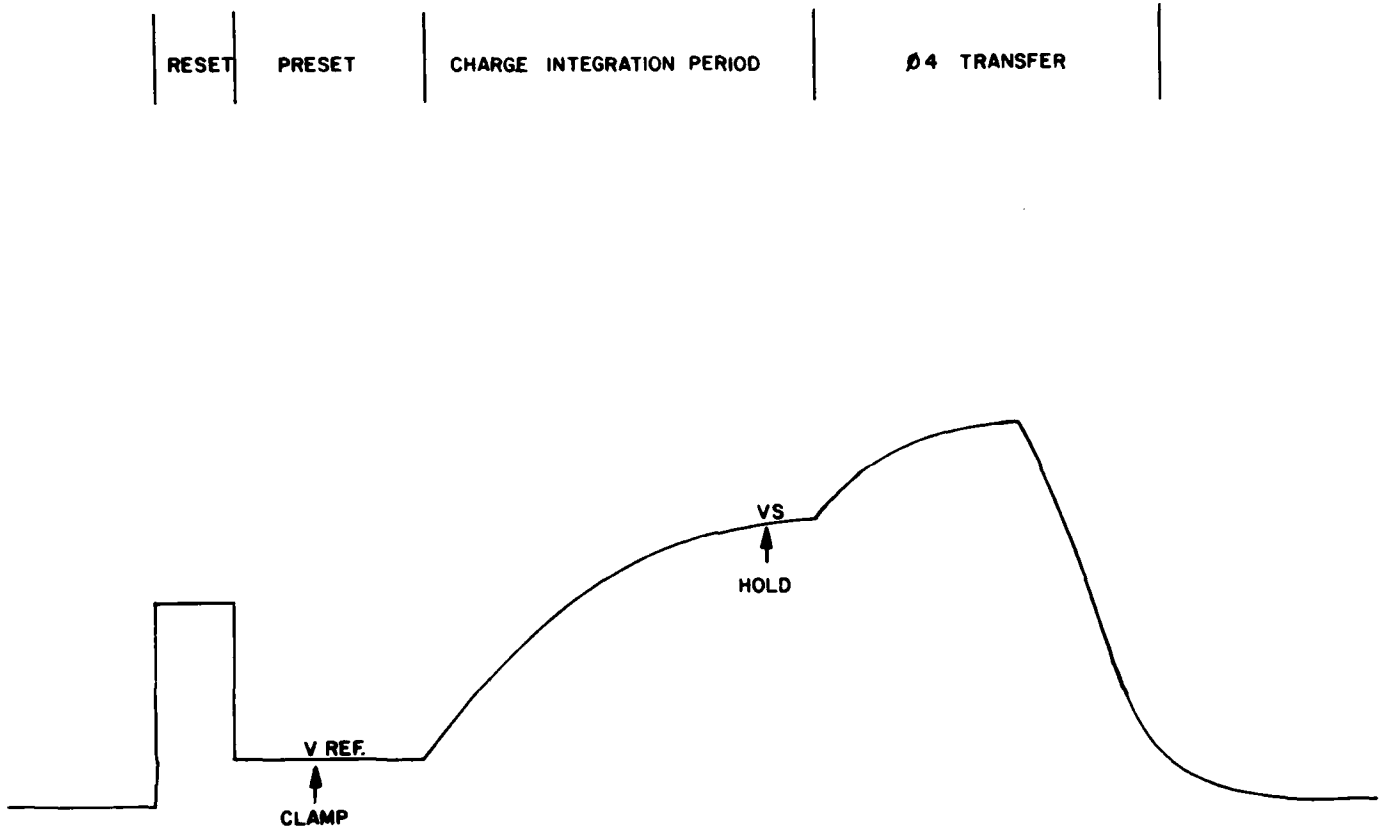


Figure A-10. One Cycle CCD Output Waveform

APPENDIX B

Test Bed Set-Up Procedure*

STEP	OPERATION
1	Place the 2708 PROM, which has been programmed with the filter weighting coefficients, into the front panel socket of the PTF Exerciser Module.
2	Connect the Master Clock to the PTF Exerciser Module.
3	Set up the PTF Module input switches, S_A and S_B, in accordance with Table B-1 for the desired mode of operation. The switches are located behind the right side panel of the PTF Module (refer to Figure 6).
4	Install cable(s) between the PTF A(B) Module and the PTF Exerciser Module.
5	Turn the system power on.
6	Place the PTF Select switch in either the PTF A or BOTH position. (NOTE: The mode load is independent of this switch. The same mode will always be programmed into both devices when using two PTF Modules).
7	Place the Coefficient/Mode switch in the MODE position.
8	Select the desired mode using the Mode Thumbwheel.

* Refer to figure 8 for a picture of the PTF Exerciser front panel.

STEP	OPERATION
9	Depress the Mode Latch (ML) pushbutton to enter the mode into the PTF(s).
10	Place the Coefficient/Mode switch in the COEF position.
11	Select the coefficient block in memory using the COEF BLOCK Thumbwheel.
12	Depress the Clear (CLR) pushbutton to initialize the module counter circuits.
13	Depress the ENTER pushbutton to program the coefficients.
14	If two PTF Modules are to be used with different coefficients, place the PTF select switch to the PTF B position.
15	Repeat steps 10 through 13.

Table B-1

PTF Module Input Switch Set-up

Mode	Switch S_A	Switch S_B
Single (1-4)	2 (↓)	2 (↓)
Dual (5-7)	1 (↑)	2 (↓)
Quad (8-9)	1 (↑)	1 (↑)
Invalid	2 (↓)	1 (↑)


DAT
FILM